Tuesday Afternoon, October 26, 1999

Electronic Materials and Processing Division
Room 608 - Session EM-TuA

High Dielectric Constant Materials and Thin Oxides

Moderators: Y.J. Chabal, Bell Laboratories, Lucent Technologies, K.T. Queeney, Bell Laboratories, Lucent Technologies

2:00pm **EM-TuA1 Challenges in Gate Dielectric Scaling**, ***D.P. Monroe***, *B.E. Weir, M.A. Alam, J. Bude, P.J Silverman, T. Sorsch, M.L. Green, A. Ghetti, Y. Ma, Y. Chen, F. Li,* Bell Labs, Lucent Technologies **INVITED**

Extrapolation of current trends in CMOS suggest that the gate dielectric of 2010 will have a capacitance equivalent to <15Å of SiO@sub 2@, including the nonzero thickness of the charge sheets in gate and substrate. It must withstand penetration of elements such as Boron during processing, and of electrons and holes during operation. It must tolerate damage from highly energetic carriers excited by the voltages on gate and drain over a multi-year operating life. Proposed replacements for SiO@sub 2@ must also demonstrate materials compatibility with the Si substrate and the gate material (currently also Si). The successful candidate will have a fewer than one interface defect for 10,000 atoms, and a uniformity across wafers, lots, and runs of better than 10% (3@sigma@). We will discuss these daunting materials and processing challenges from a transistor and circuit perspective, concentrating on the capacitance, mobility, boron penetration, and time-dependent dielectric breakdown of SiO@sub 2@ and nitrided oxides thinner than 30Å, as measured by ellipsometry. The electrical thickness of such oxides is thicker by at least 5Å, depending strongly but reproducibly on the oxide field. Simple measurements of this dependence are critical to understanding the transistor drive capability and the leakage current. The breakdown properties are more strongly governed by the applied potentials than the field. However they are strongly sensitive to the polarity of the gate voltage, even after care has been taken to include the large effects of band bending. This indicates the important role of the carrier dynamics in the anode. The "soft" breakdown of these thin oxides indicates a reduced role of positive feedback that results in higly conductive filaments in thicker oxides; indeed, some transistors continue to function even after "breakdown." We will outline some ideas for the physical mechanisms underlying the special properties of breakdown in these films.

2:40pm **EM-TuA3 Investigation of Titanium Nitride Gates for Tantalum Pentoxide and Titanium Dioxide Dielectrics**, ***D.C. Gilmer***, *C.C. Hobbs, L. La, B. Adetutu, J. Conner, M. Tiner, L. Prabhu, S. Bagchi, P. Tobin,* Motorola

The continuing push to decrease the feature size of microelectronic devices is hampered by some of the physical properties of the current materials. According to the National Technology Roadmap for Semiconductors (NTRS) projections, deep sub-micron device scaling indicates that silicon dioxide gate dielectrics must be scaled to less than 25 angstroms. It is generally accepted however, that such scaling will not be practical due to the rapid increase in tunneling current and resultant decrease in lifetime for these very thin silicon dioxide gate dielectrics. One alternative is to replace silicon dioxide with a material having a higher dielectric constant that will allow the use of thicker, less leaky, films. Towards this end, compounds such as tantalum pentoxide and titanium dioxide have been evaluated to replace silicon dioxide as a gate dielectric. Poly-silicon, currently used as the gate metal in MOSFETs, has been shown to react with transition metal oxides such as tantalum pentoxide and titanium dioxide to form an undesirable interfacial layer between the poly-silicon and metal oxide. Due to this incompatibility of poly-silicon metal gates with tantalum pentoxide or titanium dioxide gate dielectrics, an alternate metal gate material will need to be adopted for these alternative gate dielectrics. Titanium nitride (TiN), a mid-gap metal, has been extensively studied (and used) as a barrier material in many microelectronic devices. This paper reports on the investigation of physical vapor deposited and chemical vapor deposited titanium nitride for the application of a gate metal in capacitors (with sidewall spacers) using tantalum pentoxide or titanium dioxide as the gate dielectric. Electrical characteristics from C-V and I-V data, along with high resolution transmission electron microscopy of the TiN/gate oxide interface, for as-deposited and thermally annealed samples will be reported.

3:00pm **EM-TuA4 Separate and Independent Reductions in Direct Tunneling in Oxide/Nitride Stacks with Monolayer Interface Nitridation Associated with the i) Interface Nitridation and ii) Increased Physical Thickness**, ***Y. Wu***, *H. Niimi, H. Yang, G. Lucovsky,* North Carolina State University

Reduction of direct tunneling in aggressively-scaled CMOS devices with deposited oxide/nitride stacks and/or oxynitride alloys is crucial for replacement of thermally-grown oxides. We have identified two separate and independent mechanisms for tunnel current reduction that have been combined in oxide/nitride stacks with monolayer interface nitridation to yield current densities <10@super -2@ A/cm@super 2@ for stacks with oxide-equivalent thickness <1.6 nm. Fabrication of these stacks combines remote plasma-assisted nitridation and deposition processes to independently control nitrogen concentration profiles at the atomic layer level at interfaces and in bulk films. The order of interface nitridation is crucial and monolayer concentrations to reduce direct tunneling by ~ten require two 300°C steps: i) first, remote plasma-assisted oxidation of H-terminated Si(100) to form a ~0.6 nm passivating oxide, followed by ii) remote plasma-assisted nitridation to insert a monolayer of N-atoms at the Si-interface. XPS results indicate that the reduction in tunneling derives from differences in interfacial suboxide bonding associated with nitridation. Since tunneling increases exponentially with decreasing film thickness, incorporation of nitride layers in O/N stacks allows use of physically thicker films while maintaining capacitance equivalent to thinner oxides. We find that increases in thickness are in part mitigated by decreases in the product of the tunneling mass and thickness-averaged-barrier-height in the nitrides, limiting tunneling decreases to ~10-20 with respect to single layer oxides. However, using remote plasma-assisted processing to separately control interfacial and bulk dielectric nitrogen profiles, it has been possible to combine these two order of magnitude decreases and achieve reductions in tunneling of more than 200 in N/O/N stacks. These have been included in NMOS- and PMOSFETs which display excellent current drive and high reliability.

3:20pm **EM-TuA5 High K Gate Dielectrics for Sub-100nm CMOS**, ***D.L. Kwong***, University of Texas, Austin **INVITED**

With the scaling down of device dimensions, conventional SiO2 and oxynitride films will reach their physical limits in terms of thinning. As a result, there has been a great interest in the development of high permittivity materials as MOS gate dielectrics for sub-100nm CMOS. In this talk, the requirements and significant challenges in developing high K gate dielectrics with performance and reliability specs consistent with NTRS roadmap are reviewed. Results will be presented to demonstrate the importance of the interface layer at highK/Si interface. The choice of high K materials and issues associated with process integration for sub-100nm CMOS will also be discussed.

4:00pm **EM-TuA7 Evidence of Aluminum Silicate Formation at the Al@sub2@O@sub3@/Si Interface for Thermal and Plasma Enhanced Chemical Vapor Deposited Al@sub2@O@sub3@ Thin Films**, ***D. Niu***, *T.M. Klein, G.N. Parsons,* North Carolina State University

An important issue in the determination of a suitable high k gate dielectric for advanced CMOS device is the stability of the material with the Si substrate. An insulator with a covalent nature, a limited number of oxidation states and a resistance to ionic transport would be an attractive candidate for this application. This paper investigates the properties of thin Al@sub2@O@sub3@ films as a possible higher-k (12~15) alternative to SiO@sub2@. The films were formed in a 6" compatible triode plasma reactor which was also used for thermal CVD. A variety of aluminum precursors were studied, including Al acetylacetonate, Al sec-butoxide, and Al isopropoxide. A new liquid precursor, triethyl-dialuminum tri-sec-butoxide was also tested. The new precursor is safe, easy to handle and does not decompose with prolonged heating at 150°C. O@sub2@, N@sub2@O and H@sub2@O were used as oxygen sources in both plasma and low temperature (300-400°C) thermal deposition. In the thermal process, H@sub2@O resulted in deposition rates >10 Å/sec, with Ea=0.16 eV, compared to 0.1 Å/sec and Ea=1.1 eV for O@sub2@ precursor. IV, CV, TEM, ellipsometry and nuclear reaction profiling were used to characterize thin (20-300 Å) Al@sub2@O@sub3@ films on silicon. The films show acceptably low leakage current, 3X10@super-5@ A/cm@super2@ at 1 V for a 5 nm thick film. In some process conditions, clear evidence for mixing of aluminum oxide and silicon is observed in the capacitance measurement, consistent with the optical and structural evaluations. A fit of the capacitance data to a simple model is used to predict the dielectric constant of aluminum silicate layer.

4:20pm **EM-TuA8 Thermally Grown Gate Insulators for Heterostructure p-MOSFETs**, ***D.W. Greve***, *A.C. Mocuta,* Carnegie Mellon University

With decreasing channel length and increasing channel electric field, it is increasingly difficult to maintain adequate transistor ON currents in scaled MOS technologies. Germanium-silicon heterostructure p-MOSFETs potentially offer improvements in channel mobility of 30-50%; however, devices with thick channels and high germanium fraction may relax during thermal oxidation or other subsequent high-temperature processing. We have fabricated heterostructure MOSFETs and MOS capacitors using germanium-silicon-carbon epitaxial layers grown by UHV/CVD. We will show that low-carbon Si@sub 1-x-y@Ge@sub x@C@sub y@ channels do not relax for thermal anneals as high as 900 C. Consequently it is possible to use a thermally grown gate SiO@sub 2@ gate insulator while still maintaining a high channel charge capacity in the Si@sub 1-x-y@Ge@sub x@C@sub y@ layer. This has been demonstrated using heterostructure MOS capacitors with 30 nm Si@sub 1-x-0.002@Ge@sub x@C@sub 0.002@channels in which the germanium fraction x has been linearly graded from x=10% to x=40%. For cap layers approximately 6 nm in thickness after gate insulator growth, germanium surface segregation during epitaxial layer growth leads to a poor quality insulator-semiconductor interface. However, for thicker cap layers nearly ideal MOS C(V) characteristics are observed. We will also report on heterostructure p-MOSFETs which have been fabricated with Si@sub 1-x-y@Ge@sub x@C@sub y@ channels and thermally grown gate insulators. It will be shown that these devices exhibit channel mobilities of 200 cm@sup 2@/Vsec at room temperature, which is comparable to that reported with Si@sub 1-x@Ge@sub x@ channels and plasma silicon dioxide gate insulators. This demonstration opens the way toward the application of heterostructure p-MOSFETs in practical CMOS technologies.

4:40pm **EM-TuA9 Deposition of ZrO@sub 2@/SiO@sub 2@ Alloys by 300° Remote Plasma Processing for Alternative High-K Gate Dielectrics in Aggressively Scaled CMOS Devices**, ***R. Therrien***, *B. Raynor, D. Wolfe, G. Lucovsky,* North Carolina State University

Stimulated by targeted performance goals for aggressively-scaled CMOS devices, there has been much interest in alternative gate dielectric materials to replace SiO@sub 2@. The choice of materials is based on identifying insulating oxides with dielectric constants greater than SiO@sub 2@, so that physically-thicker films, anticipated to have reduced direct tunneling, will be equivalent to thinner oxides. This paper describes the deposition of ZrO@sub 2@/ SiO@sub 2@ alloy films by 300°C remote plasma-assisted CVD. This approach has two potential advantages with respect to conventional thermal CVD. First, by injecting the Zr precursor, Zr(IV) t-butoxide, and the Si precursor, silane, downstream from the plasma region, and driving the CVD reaction with active O-species extracted from an upstream O@sub 2@/He plasma, complete oxidation of Zr and Si has been confirmed by on-line AES and off-line FTIR. Films prepared in this way are amorphous as-deposited, as determined from FTIR and electron diffraction, and more importantly remain amorphous up to at least 900°C after annealing in an inert ambient. This paper describes the deposition process, and identifies the way in which the relative concentration of ZrO@sub 2@ to SiO@sub 2@ has been controlled to achieve deposition of films approaching the compound ZrSiO@sub 4@ composition. Other properties of these films relative to their role as a replacement dielectrics are discussed; e.g., optical studies of the band-gap, and electrical capacitance-voltage and current-voltage characteristics are presented. These allow us to obtain i) the static dielectric constant, ii) the conduction band offset energy with respect to Si and iii) the tunneling electron mass. Based on these measurements, ZrO@sub 2@/SiO@sub 2@ alloys in conjunction with hyper-thin (~0.5 nm), nitrided SiO@sub 2@ interfacial layers can be used to scale the oxide-equivalent dielectric thickness down to about 1 nm.

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