Manufacturing Science and Technology Group
Room 317 - Session MS-MoA

Contamination Free Manufacturing

Moderator: A.C. Diebold, Sematech

2:00pm **MS-MoA1 Green House Effect and LSI Process Technology**, ***K. Okumura***, *T. Ohiwa,* Toshiba Corporation, Japan **INVITED**

While LSI devices contribute to saving energy, their fabrication consumes large amounts of electric power and PFC gases. This paper will discuss the new LSI process technology to alleviate such negative aspects. Among the process tools, especially the furnaces and dry pumps consume a large quantity of electric power. The fast temperature processor (FTP), which realizes ramp temperature up and down at high speed, succeeds in maintaining temperature at 300 - 400 °C and ramping up to 800 - 900 °C only when processing. This leads to a 30 - 50 % power reduction compared to the conventional furnace which constantly maintains its temperature at 800 - 900 °C. Dry pumps with an inverter controlled DC motor drive consume half as much power as conventional induction motor drive systems. Furthermore, quick response of the DC motor without over-current makes it possible to turn it on only when necessary and off during machine idling, which leads to 15 - 80 % less power. In RIE and CVD machines, as much as 10 - 15 SLM of purge N@sub 2@ gas is used in order to prevent clogging of dry pumps by by-products. Pure N@sub 2@ gas generation also requires a vast amount of electric power. Therefore, reduction of N@sub 2@ gas is another effective approach. A dual in-line cold trap was newly developed for this. It consists of two traps. One traps by-products before the dry pump, and the other can be flashed meanwhile. Improving the efficiency of gas usage leads to reduction of PFC consumption. A new gas circulation system was developed, which pumps the exhausted gas still containing usable process gas into the RIE reaction chamber to be reused. Because many kinds of PFC gases after plasma processing eventually change to the most stable CF@sub 4@ gas, recycling of CF@sub 4@ gas is a key point. We have developed a dual trap system which operates at liquid N@sub 2@ temperature. It is capable of trapping CF@sub 4@ gas exhausted from an RIE reaction chamber. This system has the possibility of distillation of PFC gas by the appropriate control of regeneration temperature.

2:40pm **MS-MoA3 Ultra-Low-Temperature Growth of High-Integrity Silicon Oxide and Nitride Films by High-Density Plasma with Low Bombardment Energy**, ***K. Sekine***, *R. Kaihara, Y. Saito, M. Hirayama, T. Ohmi,* Tohoku University, Japan

As semiconductor devices are scaled down to smaller dimensions, conventional processing temperature such as 900°C will be incompatible with the desired device structure. For example, conventional high-temperature gate insulator formation process changes the impurity profile previously formed in the substrate. Moreover, it is necessary to introduce metal substrate SOI device for future high speed (>1GHz) ULSI device. To realize the metal substrate SOI device, all of manufacturing processes have to be done at below 550°C. Thus gate insulator also must be formed below 550°C. Therefore lowering growth temperature of high-integrity gate insulator is a key for future metal substrate SOI device fabrication. High integrity ultra-thin silicon oxide and nitride films can be obtained at 430°C by direct oxidation and nitridation of silicon surface. Such a low temperature oxidation and nitridation could be realized by employing newly developed high-densit!y plasma system with low ion bombardment energy less than 7eV and high plasma density above 10@super12@cm@super-3@. The electrical properties of these films are nearly the same level as those of thermally grown films. This technology becomes very promising for fabricating feature metal substrate SOI devices and silicon nitride gate MISFET.

3:00pm **MS-MoA4 Low-Temperature Large-Grain As-Deposited Poly-Si Formation by Microwave-Excited PECVD Using SiH@sub 4@/Xe**, ***W. Shindo***, *S. Sakai, T. Ohmi,* Tohoku University, Japan

We have achieved as-deposited large-grain polycrystalline silicon at a temperature of 300°C by plasma enhanced CVD using SiH@sub 4@/Xe. The grain size evaluated by X-ray diffraction is 25nm, which is believed to be the largest grain size among 100nm-thick as-deposited poly-Si films fabricated by various methods at low temperature. High-density (>10@super 12@cm@super -3@) plasma having very low electron temperature (approximately 1eV) excited by microwave irradiation was used for the film growth. Plasma density and electron temperature dominate ion flux density and ion kinetic energy incident on the substrate surface, respectively. Thus, high-flux and low-energy ion bombardment (

3:20pm **MS-MoA5 Balanced Electron Drift Magnerton Plasma Source for Uniform SiO@sub 2@ Etching**, ***R. Kaihara***, *T. Ohmi,* Tohoku University, Japan*; H. Komeda,* Sharp Corp., Japan*; Y. Hirayama,* Tokyo Electron Yamanashi Ltd., Japan*; M. Hirayama,* Tohoku University, Japan

Magnetron etcher using dipole ring magnet has demonstrated its high selectivity with lower micro-loading effects. When parallel magnetic field is applied by dipole ring magnet, the uniformity V@sub dc@ and ion flux is degraded by ExB drift of secondary electrons on the wafer. The inherent non-uniformity causes crucial problems such a charge up damage and etching non-uniformity. In order to improve non-uniformity of V@sub DC@, gradient magnetic field has been employed in a magnetron etcher using dipole ring magnet. Almost uniform V@sub DC@ profile can be achieved by optimizing the magnetic field profile. Even though optimizing magnetic field profile is effective, there is some problems such as restricted process window and non-uniformity of ion flux. On the other hand, we applied RF(100MHz) to upper annular electrode in order to improve non-uniformity of V@sub DC@ and ion flux. The electron drifts can be balanced between the upper annular electrode and the lower electrode. Uniformity of V@sub DC@ (±4V) and ion flux (±3%) are simultaneously obtained by the balanced electron drift (BED) magnetron etcher. Excellent etching profile of 0.15µm contact hole is also obtained uniformly on 200mm wafer.

3:40pm **MS-MoA6 Influence of Wafer Back Surface Finish on Dry Etching Characteristics**, ***S. Muramatsu***, *K. Ando, H. Nanbu, H. Miyamoto, T. Kitano,* NEC Corporation, Japan

Process tolerance and controllability have become more severe with the scaling down and integration of devices. Wafer back surface finish is a factor affecting the process conditions such as dry etching and rapid thermal annealing. In this study, the correlation between back surface roughness and dry etching characteristics was investigated. The back surface roughness was changed from Ra=0.41 nm to 50.1 nm by final back surface treatments (mechanochemical polishing or chemical etching). Contact-hole etching with CHF@sub 3@ gas was performed for interlayer CVD oxide deposited on the front surface of wafers. The etching rate for a smooth back surface (0.41 nm) was increased by 1.1 times over that for a rough back surface (50.1 nm). During contact-hole etching, the wafer temperature of the smooth back surface was10°C lower than that for the rough back surface. This is due to the difference in electrostatic chucking (Ra=80-120nm) force during contact-hole etching. When the smooth back surface wafer was used, the adhesion area between the dry-etching stage and the wafer back surface increased because the back surface roughness was small. Consequently, the wafer can be cooled down sufficiently and the etching rate dominated by gas absorption was increased. As well as the etching rate, the position where residual gas was deposited inside the contact hole was governed by the degree of the wafer back surface finish. These experimental results indicate that the roughness of the wafer back surface should be well controlled for fabricating advanced devices.

4:00pm **MS-MoA7 Precise Control of Gas Ratio in Process Chamber**, ***Y. Shirai***, *O. Nakamura,* Tohoku University, Japan*; N. Ikeda, R. Dohi,* Fujikin Inc., Japan*; T. Ohmi,* Tohoku University, Japan

In 300mm wafer generation, many kinds of single wafer processing will be necessary to establish higher process uniformity on a wafer. For achieving low cost production, it is necessary high-rate processing such as wafer/min including load-unload time. Process gas distribution system is one of the most critical issues for process uniformity and high-rate processing. Especially, high quality and uniformity of film formation process strongly depends on initial gas distribution in a process chamber. We have developed advanced integrated gas system and studied process gas ratio in process chamber using FT-IR method. We have prepared two types of integrated gas distribution system. One is the conventional system consists of MFC and air operate valve, the other is the advanced system consists of new pressure flow controller with electric valve. This new pressure flow controller built on the principle that the flow rate is directly proportional to the upstream pressure if the upstream pressure is more than two times of downstream pressure. We have introduced three kinds of process gases into a process chamber. The conventional system shows over shoot phenomena. The process gas concentration increase more than two times of the steady state. In addition, it takes more than 20 seconds to be steady state of gas ratio and chamber pressure after the valve operation. On the other hand, the advanced system does not show over shoot phenomena. The steady state of gas ratio and chamber pressure can be obtained within 2 seconds after the valve operation.

4:20pm **MS-MoA8 Clean Aluminum Oxide Formation on Surface of Aluminum Cylinder in an Ultraclean Gas Sampling System**, ***Y. Ishihara***, *N. Itou, T. Kimijima, T. Hirano,* NIPPON SANSO Corporation, Japan

Because it is difficult to obtain enough space for a gas-analysis system in semiconductor manufacturing lines, gas purity is usually confirmed by an ex-situ analysis of gas sampled inside the gas-sampling cylinder (sampler). In order to analyze a trace impurities, it is necessary to significantly reduce the contaminants generated in sampler and to fabricate a surface and/or material with an extremely low outgassing rate. We have produced a sampler made of pure Al produced during plasma oxidation in 3% O@sub 2@/Ar after the EX process.@footnote 1@ Nevertheless, the H@sub 2@ concentration in N@sub 2@ or Ar sealed at 0.58MPa in the sampler increased from below 1ppb to 8ppb after 168hours. The CO and CO@sub 2@ concentration in O@sub 2@ also increased. Wet cleaning was carried out in the sampler in the plasma oxidation state by DI water for 72hours at a flow rate of 2L/min. After wet cleaning, the sampler was annealed at 423K for 72 hours in N@sub 2@ without exposure to air. We have confirmed that amorphous @gamma@-Al@sub 2@O@sub 3@ film with a thickness over 0.5μm was formed on the inner surface of the sampler using cross-sectional TEM observation. We have observed that the H@sub 2@ concentration in Ar or N@sub 2@ was maintained below 1ppb, the detection limit of the GC, for 168hours. The CO and CO@sub 2@ concentration in O@sub 2@ were also sufficiently low. These results suggest that the amorphous @gamma@-Al@sub 2@O@sub 3@ film formed by a series of treatments as already mentioned function as a gas-barrier film with an anti-catalytic property. @FootnoteText@ @footnote 1@H. Ishimaru, J.Vac.Sci.Tech., A7(3) 2439 (1989)

4:40pm **MS-MoA9 Gradational Lead Screw Pump Development**, ***K. Ando***, T.D.Giken Co., Ltd., Japan*; I. Akutsu,* DIAVAC Limited, Japan*; T. Ohmi,* Tohoku University, Japan

Because the silicone device industry is innovating their production processes toward the larger wafer size and the higher process speed, a vacuum pump is required higher pumping speed through ranges of the both viscous and molecular flow. There has been no known conventional pumps that have been developed so as to vacuum a chamber down to 0.01 Torr with stable exhaust velocity over the entire region including the molecular flow region. All of them provide stable pumping speed only down to 0.1 Torr. The "GLS Pump" unlike these conventional pumps demonstrated the high pumping capability of 0.0004 Torr and the pumping speed of 3600L/M over the viscous and molecular flow ranges. The improved performance is attributable to the GLS employed for the rotor design. The pump utilizes a small amount of oil. The mass analyzer test(max. mass number 120) revealed that there is no evidence of the reverse diffusion in the pressure range above 0.002 Torr with a small amount of N2gas injected. In summary, the GLS Pump has enough displacement and large intake conductance. Low reverse diffusion is in practical operation. The pumping speed is high. The power consumption is low. The byproduct is transferred and ejected from the exhaust port through the operation mechanism. The radical deposit is minimized if the case temperature is maintained at 150°C. Although manufacturing this pump requires high level of skill, the pump structure is rather simple and the maintenance is easy hence it will increase the mean time between maintenance and reduce the maintenance cost. The detail report will be prepared on the characteristics of the GLS, the pump structure, and the performance attributes.

5:00pm **MS-MoA10 Etching and Cleaning of Silicon Wafers using HF Vapor Process in the Non-Condensed Etching Regime**, ***Y.-P. Han***, *H. Sawin,* Massachusetts Institute of Technology

We have studied oxide etching mechanisms of HF vapor etching process in two regimes: the condensed regime (liquid phase) and the non-condensed regime (gas phase). In the condensed regime, the etching rate of oxide is greatly affected by the flow rate of the reactant stream and the total pressure of reactor, which can change the mass transfer rates of both reactants and products. The rate limiting steps of the etch rate have been studied at various conditions by changing the temperature of the reactor, the partial pressure of the reactants and the flow rate. The etching rate of oxide in the non-condensed regime was mainly limited by the surface reaction rate at higher temperature, but the mass transfer rate became more important at lower temperature. We also have investigated the cleaning of Na from silicon wafer in HF vapor process. It was observed that Na contamination on thick thermal oxide films was typically removed by HF vapor process. On thinner oxide films, i.e. 1-2 nm native oxide, only part of the contaminated Na was typically removed by this process. The addition of SiF4 to the HF/H2O process, i.e. HF/H2O/SiF4 was found to improve the cleaning efficiency of Na from silicon surfaces. The volatile product is believed to be Na-OSiF3.

Manufacturing Science and Technology Group
Room 317 - Session MS-TuM

Overview: Integration for Manufacturing

Moderator: J.J. Sullivan, MKS Instruments, Inc.

8:20am **MS-TuM1 Reaction/Annealing Pathways for Forming Ultrathin Silicon Nitride Films for Composite Oxide-Nitride Gate Dielectrics with Nitrided Crystalline Silicon-Dielectric Interfaces for Application in Advanced CMOS Devices**, ***G. Lucovsky***, North Carolina State University **INVITED**

Aggressive scaling of CMOS devices requires gate dielectrics with oxide equivalent thicknesses of ~1 nm by 2012. Direct tunneling is a limitation in FETs when oxide thicknesses are reduced to <2 nm. In addition, boron diffusion from p+ poly-Si gate electrodes in PMOS FETs leads to additional electrical problems for oxide thicknesses <4 nm. Interfacial nitridation improves reliability in NMOS FETs; however, it is not effective in PMOS FETs due to of boron pile-up at the Si-dielectric interface. One solution to these problems is the integration of composite oxide-nitride composites with nitrided interfaces; NON dielectrics, into CMOS devices. The paper discusses: i) deposition of hydrogenated silicon nitride by remote plasma-enhanced chemical-vapor deposition (RPECVD); ii) characterization of plasma-deposited nitrides by IR and AES; and iii) effects of post-deposition annealing on the bonded-H content. Formation of nitride thin films for NON composite dielectrics requires two process steps: i) deposition of a hydrogenated silicon nitride film at 300°C by RPECVD, followed by ii) rapid thermal annealing in an inert ambient at 900°C. During the anneal H-atoms are evolved from near-neighbor SiH and SiNH bonds, and the resulting Si and N-atom dangling bonds combine to form new SiN bonds accounting for the device-quality electrical performance. Electrical performance of devices with composite i) oxide-nitride-oxide, ONO, dielectrics, and ii) ON dielectrics with fully nitrided interfaces, NON, is discussed. For example, we demonstrate that approximately 2 molecular layers of nitride, ~0.8 nm, at the top surface of the NON dielectric is sufficient to stop B-penetration out of p+ poly-Si gate electrodes during dopant drive-in/activation anneals. Finally, nitrides produced by the two step process are qualitatively different from CVD nitrides deposited at higher temperatures, ~500°C, and subjected to post-deposition anneals in oxidizing ambients.

9:00am **MS-TuM3 Process Mixing in Cluster Tools**, ***R.A. Powell***, Novellus Systems **INVITED**

Cluster tools are widely used in advanced microelectronic manufacturing because they offer high productivity and the ability to improve thin film and interface quality through vacuum-integrated processing. While such tools are often dedicated to a single technology such as plasma etching, PVD, or CVD, it is common to integrate a number of different process technologies within the same tool. For example, the integrated process sequence of wafer degas+ preclean + PVD Ti + PVD TiN + PVD AlCu + PVD TiN can be carried out in a PVD cluster tool without a vacuum break to deposit an AlCu interconnect line. Understanding and managing the interplay between successive steps is critical to successful process integration-which in turn has an important effect on tool performance, productivity and cost of ownership. Looking forward, there is growing interest in clustering fundamentally different deposition methods such as PVD and CVD onto a common wafer handling platform to take advantage of their complementary benefits. This talk will discuss the motivation and challenge of integrating these and other processes on advanced cluster tools with a focus on film deposition. Generic issues of mixing and matching different processes on a cluster platform will be discussed with regard to vacuum requirements, ambient purity, thermal cross-contamination, and the choice of single wafer versus batch processing. Specific examples from both PVD and CVD cluster tools will be used to illustrate the general points made.

9:40am **MS-TuM5 Process Integration Overview: Development and High Volume Manufacturing of Microprocessor Products**, ***R.A. Gasser, Jr***, Intel Corporation **INVITED**

Intel Corporation provides ~80% of worldwide demand for microprocessors. Continuing to meet this demand requires the development of high performance microprocessors using the most advanced process technology available. Meeting this demand also requires the ability to ramp the technology at high volumes in many factories at the same time. This talk will first present an overview of the economics of microprocessor manufacturing. This overview will show why it is imperative for the key participants in this industry to be able to consistently deliver both high levels of transistor performance and process integration using the most advanced equipment available. Next, there will be a review of methods for robust process design. Robust process design is key to laying the foundation for eventual process ramp. Finally, there will be an overview of methods for ramping the process technology to very high volumes, while achieving high product yields.

10:20am **MS-TuM7 Value Chain Integration**, ***P.S. Peercy***, SEMI/SEMATECH **INVITED**

Driven by continuously increasing competitive pressures from increasing globalization, the semiconductor industry has undergone major structural changes over the past few years. As recently as the early 1980s, most of the process and fabrication research and development was performed primarily in large vertically integrated companies in the industry. Mission-driven research in the central research labs and the R&D pilot lines of these companies yielded most of the technology required to keep the industry's productivity growing exponentially at a rate of 25-30% per year. Today, the semiconductor industry in the U.S. has largely stratified into systems companies, device manufacturing companies, and equipment, subsystem, component, and materials suppliers. In addition, competitive pressures and changing business conditions have shifted the focus of much of the research in the central research labs of the device companies away from fabrication equipment and processing technology. As a result, an increasing amount of the new processing equipment, process technology, and materials development comes from the supply chain today. Tomorrow, the suppliers will be expected to provide virtually all of the new processing equipment and technology required by the device manufacturing sector of the industry. With the increasing stratification of the supply chain, increased vertical communication and coordination is necessary. The efficiency of the supply chain, and the industry, can be greatly increased by close customer-supplier alliances at all levels in the supply chain. Such "value chain integration" can provide a common language for simultaneous communication of requirements to all levels of suppliers. Further, joint development of the technology permits optimization of the research and development efforts throughout the supply chain. It permits competitors to cooperatively perform the research for generic, pre-competitive technologies required for the continued advancement the technology. Additional optimization comes from relying on the expertise of suppliers at all levels in the supply chain; if the requirements are developed jointly, the expertise of suppliers of a given component or subsystem frequently permits redesign and implementation in a more cost-effective and reliable manner. We will examine value chain integration in general with examples of the benefits realized through true customer-supplier alliances, then examine application of value chain integration to the semiconductor industry.

11:00am **MS-TuM9 Factory Integration in the NTRS: Future Factory Level Issues and Needs**, ***G.M. Gettel***, SEMATECH / Texas Instruments, Inc. **INVITED**

The global challenge in the National Technology Roadmap for Semiconductors (NTRS) is to keep the semiconductor industry's productivity engine on track by staying on the 25-30% per year manufacturing cost reduction curve. The industry has been successful in the past in driving down the curve by using feature size reductions and wafer diameter increases. In the future, these two approaches will continue to be exploited but four factory level challenges will have to be addressed to keep the industry from getting derailed. The four challenges are: Escalating factory cost; Factory investment risk and time factors; Overall Factory Effectiveness; and Process / Factory complexity. Factory capital costs are escalating over time up an exponential curve. With the escalating factory costs comes escalating investment risk. Future factories will need faster design, construction, tool installation and ramp in order to pay back in a reasonable time period. Improved bottleneck and average tool OEE are needed. In the future, incoming equipment in an operation will need to have a higher initial OEE and reach maturity quicker. Processes (driven by smaller feature sizes and larger wafer diameters) and factories (driven by economy of scale) will be increasingly complex in the future. This complexity is increasing exponentially. The systems capability to deal with the complexity is evolving at a slower pace resulting in a "data overload gap". These factors drive the need for improved decision support capability. Future factories will require more tool to tool automation, better wafer and die traceability and improved material control systems. Software content in equipment is growing by more than 25% per year. To prevent this increased amount of software complexity from derailing effective factory operation, more reliable and predictable software will be

required. This presentation will review the trends, issues and potential solutions for these four difficult factory level challenges.

Manufacturing Science and Technology Group
Room 317 - Session MS-TuA

Process, Integration, and Modeling
Moderator: K. Aitchison, Novellus Systems

2:00pm **MS-TuA1 Pattern/Etch/Clean Process Interactions for 0.18um CMOS Gate Formation***, **R.J. Gale**, R. Kraft, R.T. Laaksonen, A.L.P. Rotondaro,* Texas Instruments **INVITED**

As device dimensions continue to shrink to 0.18um and below, the interaction between steps in a process flow becomes more critical. These interactions can be synergistic. In many cases, however, the processes must be co-optimized to minimize the negative effects. One of the most critical process modules in a CMOS device flow is the formation of the gate geometry. We will focus on pattern, etch, and post-etch clean interactions in forming the gate. Dry etch is used to reduce the photoresist patterned line width. This approach permits the wafer patterning to be performed in a more robust process regime thus producing less variation. Once the desired line width reduction has been accomplished, the polysilicon is dry etched, stopping on the thin (<30A) gate oxide. Finally, the remaining photoresist and etch polymer residues must be removed without stripping the thin gate oxide protecting the active regions of the device. Changes in the dry etch process to maximize anisotropy to provide vertical profiles for the gate geometry and high selectivity to gate oxide drive a more aggressive post etch clean process that also must be optimized for oxide selectivity and critical dimension control. This paper discusses the challenges and tradeoffs to successfully accomplish the 0.18um gate formation.

2:40pm **MS-TuA3 Dual Damascene : Etching Process Characterisation of "Self Aligned" and "Counter Bore" Architectures***, **P. Berruyer**, F. Vinet,* LETI-GRESSI, France*; H. Feldis,* SGS-Thomson, France*; E. Tabouret, Y. Trouillet,* LETI-GRESSI, France*; Y. Morand,* SGS-Thomson, France

One of the main challenges of the next few years is the improvement of interconnect performances, namely integration density and dynamic performances. This can not be done without combining improvement in both design and technology. In term of technology, different ways are explored : introduction of low k dielectric and low resistivity metal. Concerning low resistivity metal, copper seems to be the best candidate to replace AlCu. But the main disadvantage of this material is its high resistance to plasma etching. Taking into account that copper is highly resistant to plasma etching, that Chemical Mechanical Polishing processes are available and that dual damascene architecture can significantly increase interconnect density, copper is usually introduced in a damascene architecture. Among the different ways of achieving dual damascene structures, two of them, called " self aligned " and " counter bore " have to be taken into account. In this paper we will first describe the process steps of these two architectures. We will point out that both architectures require the development of a specific high aspect ratio dielectric etching process with high selectivity to nitride. A medium density reactor (TEL Unity DRM) will be used for the experiments. Different process conditions will be applied to dual damascene structures for a morphological characterisation. Major attention will be paid on selectivity to nitride, microloading, etch stop and CD control. Etch rate and selectivity to photoresist will also be studied. The architectures and the etching processes will be compared on an electrical lot with copper metallisation. Contact resistance and yield on 10 million contact chains will be measured. The advantage and drawbacks of each architecture will be discussed with regard to etching processes. An optimised dual damascene process will be proposed.

3:00pm **MS-TuA4 Low k Polymer Etching for Dual Damascene Technology Application to SILK Material***, **F. Vinet**, E. Tabouret,* LETI-GRESSI, France*; Ch. Vivensang,* Tokyo Electron Europe LTD, France

Scaling down of interconnect requires a change in architecture and materials to be integrated. Dual Damascene scheme in combination with copper as metal conductor, appears to be the most acurate choice for sub 0.18 µm design rule technology. The dielectric material necessary for this application is still under improvement to achieve the required properties such as, dielectric constant<2, thermal stability and good adhesion on mineral or organic layers. The most advanced materials are based on polymers. In order to etch these materials, a hard mask is necessary due to their poor resist selectivity (1:1).Silicon dioxide (SiO2)is the most commonly used hard. Depending on the polymer composition, the compromise between high aspect ratio and mask erosion has to be found. Among the different available materials, SILK from Dow Chemicals, presents a chemical stability compatible with the thermal budget of our current technology. Moreover, this material is purely organic and contents no silicon; in this case an etching chemistry without fluorine can be used, ensuring a good selectivity to the hard mask. The etching properties, as well as the requirements related to the use of a Dual Damascene architecture have been investigated in this paper. A 1500Å thick SiO2 hard mask was deposited on top of 1µm spin coated SILK. By using DUV lithography 0.225 µm holes and 0.3/0.3 µm L/S patterns were defined. A medium density etcher from TEL, DRM85 UnityII was used for the experiments. By using a pure O2 chemistry, an overhang between hard mask and SILK is observed ; moreover due to isotropic etching, the sidewalls after etching are bowed. In order to overcome these effects, different chemistries have been tested in combination with etching process parameters to form a passivating layer. With optimised conditions, 0.225 µm holes were obtained with straight profiles. In our experiments, the limitation for higher aspect ratios is due to lithography and not to etching conditions. Whatever the Dual Damascene structure is used, successive steps of fluorinated and non fluorinated chemistry has to be used to etch alternatively SiO2/SILK/ SiO2.The effect of such a sequence has been studied on the etched profiles as well as the influence of reactor fluorine memory effect. Optimised conditions for both, process and reactor, are proposed to ensure a reliable process for sub 0.18µm technology.

3:20pm **MS-TuA5 Manufacturing Issues for MEMS Production***, **K.W. Markus**,* MCNC **INVITED**

As the commercial and military implementation of MEMS technology solutions moves further up the line from research to consumer and commodity applications, the need for a robust manufacturing technology base for MEMS continues to increase. MEMS, the merging of computation with sensing and actuation into an integrated system-based solution for problems pertaining to the physical world, has benefited greatly and grown rapidly out of the widespread infrastructure developed in the U.S. for the manufacture of integrated circuits (IC). The U.S. approach to MEMS applies the repetitive layering, batch-processed wafer methods of the integrated silicon circuit manufacturing industry to achieve revolutionary strides in mechanical miniaturization and system integration. This outgrowth from the IC industry has both benefits and pitfalls, and it is going to be capitalizing on the benefits and navigating the pitfalls that will determine the success of the transition of MEMS from its current low or sporadic volumes to the high-volume successes that will demand large-scale production capabilities. One of the many benefits that MEMS derives from its common base with the IC industry is the methodology behind its fabrication sequences. Most MEMS processes can be decomposed to a repeating series of material deposition, patterning and subsequent removal of specific areas of the material. This layering is repeated until the basic structure is created either on or within the silicon wafer. While many of these steps, or unit processes, are similar to those used in IC processing, the mechanical nature of MEMS puts additional stringent requirements on the processes that do not exist in the IC processes. Beyond the fabrication of the basic wafer structure, the releasing of the structures, the handling of these released wafers or die, the packaging, and the testing of the MEMS devices all can challenge even the most sophisticated and technically advanced manufacturing line. While there is a strong and vibrant manufacturing infrastructure for the IC industry, the uniqueness of some of the key steps of MEMS technology challenge the existing manufacturing technology infrastructure and place challenges and potential limitations on the development of a comparable support-structure for MEMS. Much of the IC industries infrastructure has grown as a result of, and not in advance of, the explosive growth the IC industry in the last 15 years. While the outlook for MEMS is quite strong ($9B - $30B by 2000)@footnote 1@ , it is a mere trifle when compared against the $148B@footnote 2@ (1995) IC market (year 2000 projection $371B) . MEMS will need to find creative and unique ways to ensure that the level of attention necessary to help drive the growth of manufacturing infrastructure are found and nurtured, despite the overwhelming shadow of the IC market. This presentation will discuss the manufacturing issues affecting the growth of MEMS from commercial curiosity to manufacturing reality, including design and simulation tools, fabrication equipment, through-put and resources, packaging, testing and reliability. @FootnoteText@ @footnote 1@ Micromachine Devices newsletter, August 1997 @footnote 2@ World-wide Merchant Semiconductor Forecast, Source: ICE, Status 1996

4:00pm **MS-TuA7 Design of a 300 mm CVD Tungsten Reactor using Computational Fluid Dynamics**, ***E.J. McInerney***, *T.M. Pratt, A. Tahari,* Novellus Systems

Over the next several years, the semiconductor industry will transition to 300 mm wafers for IC fabrication. To support this shift, the semiconductor equipment companies must develop 300 mm processing tools that are both manufacturing worthy and cost effective. In the past, designing equipment for larger sizes was primarily a matter of scaling the components: chamber, showerheads, heaters, etc. For batch systems, often the batch size would also be reduced to minimize the gain in footprint. However, as capital equipment costs become an increasing fraction of wafer fabrication costs, it becomes necessary for semiconductor equipment to not only handle larger sizes, but also to be substantially more cost effective. We report here on how computational fluid dynamics modeling was used to guide the design and development of a high throughput, 300 mm multi-station CVD tungsten reactor. Through modeling we were able to investigate novel gas-based isolation schemes that allowed the individual deposition stations to run separate processes, without cross contamination. The resulting reactor can simultaneously deposit silane reduced and hydrogen reduced tungsten films at adjacent deposition stations without the danger of gas phase nucleation or WF@sub 6@ device attack. This leads is a significant drop in the idle time of deposition stations and a large boost in throughput.

4:20pm **MS-TuA8 Computational Flow Modeling for Electrostatic Chuck Applications**, ***L.A. Gochberg***, Novellus Systems, Inc.

An electrostatic chuck used in a deposition or etching process is comprised of a ceramic material with an embedded electrode, on which a wafer is placed in the reactor chamber. The gas flow paths on the backside of the wafer can be adjusted to help control the wafer temperature. The dimensions of these flow pathways can be as small several microns, and at typical backside gas operating pressures (1-10 Torr), the flow can be anywhere between continuum and free molecular flow. Though tools are available to model these flows (Direct Simulation Monte Carlo and Navier-Stokes with slip boundary conditions), these flow conditions, typical in wafer processes, bring up some significant computational challenges. Also, the 3D nature of the real chuck flow with all its complex geometry compounds the numerical difficulties. In this paper, the focus will on a 2D approximation to the flow on the backside of the wafer, which is essentially flow between two flat, parallel circular disks. This geometry is quite similar to the 3D geometry in the electrostatic chuck, but without the complex set of gas grooves. Computations will be performed using Navier-Stokes computational fluid dynamics (CFD) with and without slip boundary conditions, Direct Simulation Monte Carlo (DSMC), and an analytical solution to the problem. These results will be compared to experimental data for helium gas flow through that same geometry. Comparisons show an excellent agreement between all the computations and the experiments in the continuum and near-continuum transition flow regime. The DSMC results and analytical solution match well with the data throughout all the flow regimes. However, the CFD with slip shows a capability in this 2D geometry to capture the trends seen in the data and DSMC out to much higher Knudsen numbers than would be typically expected. These CFD with slip results can be used as a design tool to conservatively estimate backside gas pressure distributions and reliably design gas distribution channels.

4:40pm **MS-TuA9 TEOS CVD Topography Simulation Using Surface CHEMKIN and EVOLVE**, ***A.H. Labun***, Digital Equipment Corporation; *T.S. Cale,* Rensselaer Polytechnic Institute; *P. Ho, H.K. Moffat, M.E. Coltrin,* Sandia National Laboratories

Although the pyrolysis of Si(OC@sub 2@H@sub 5@)@sub 4@ (TEOS) leads to formation of a highly reactive deposition precursor, increasing the residence time in a chemical vapour deposition (CVD) process leads to more, not less, conformal SiO@sub 2@ deposition in high aspect ratio features, contrary to the assumption of a first order deposition reaction commonly used in topography simulation. A newly developed Surface CHEMKIN interface in the EVOLVE 5.0 topography simulator allows EVOLVE to be used in conjunction with CHEMKIN-based reactor codes to explore this and other CVD reaction mechanisms and make process recommendations. Ab initio calculations and experiments lead to consideration of a network of 8 reversible, heterogeneous reactions and 3 reversible, homogeneous reactions, involving 5 surface species and 6 gasses. Under short reactor residence time conditions relatively little TEOS decomposes and it remains the dominant constituent of the bulk gas, but transport limitations cause byproduct gasses to dominate in submicron features. They promote the reverse heterogeneous reactions, slowing the deposition rate inside the features and causing nonconformal films. The sticking coefficients of TEOS and the precursor may vary substantially over the topography and during the deposition. Decomposition of the TEOS under longer reactor residence time conditions leads to similar gas compositions inside and out of the features and hence film deposition in the features becomes conformal.

5:00pm **MS-TuA10 Plasma-Induced Nitridation of the Gate Oxide Dielectrics: Linked Equipment-Feature-Atomic Scale Simulations**, ***V. Sukharev***, *S. Aronowitz, H. Puchner, V. Zubkov, J. Haywood, J. Kimball,* LSI Logic Corporation

Quantum chemical calculations were employed to get insight into the mechanisms involved in plasma-induced nitridation of gate oxide that will suppress boron penetration. The roles played by the nitrogen cations and atoms were explored. Based on these results, we assumed the following model for the nitrogen incorporation: nitrogen cations cleave bonds in substrate subsurface region; the depth of the damaged layer is determined mainly by the energy of the incident ion, binding energy of nitridated material and its density. Nitrogen atoms, whose concentration is usually several orders of magnitude greater than the cation concentrations, readily react with dangling bonds to produce @>=@Si-N- and @>=@Si-O-N- radicals. A subsequent anneal produces an appropriate condition for reaction between the above radicals and results in the nitrogen insertion into the SiO@sub 2@ ring structure. Thus the nitrogen cations play the role of the promoter for the entire SiO@sub 2@ nitridation. It was shown that B interaction with siloxane rings that contain incorporated nitrogen yielded a larger energy gain than rings without nitrogen. This explains the chemical nature of the nitrogen-induced barrier effect. Monte Carlo (PROMIS) simulations were used to simulate the necessary energy of incident N@sub 2@@super +@ cations to produce the bond cleavage down to a particular depth in the amorphous SiO@sub 2@ layer. A combination of the Hybrid Plasma Equipment Model and Plasma Chemistry Monte Carlo Simulation codes were used to simulate nitrogen atomic and cation fluxes and their angular and energy distributions at the wafer surface. Combining simulated cation energies with PROMIS Monte Carlo simulation results make it possible to derive the plasma process parameters that will permit a desired level of nitridation to be reached.

Plasma Science and Technology Division
Room 318/319/320 - Session PS+MS-TuA

ULSI Technology

Moderator: M. Liehr, IBM T.J. Watson Research Center

2:40pm **PS+MS-TuA3 Front End Integration for ULSI Technologies**, ***W.A. Mueller***, SIEMENS Microelectronics, DRAM Development Alliance, Germany **INVITED**

Key frontend integration challenges for sub 0.25 µm technologies will be discussed. For device isolation shallow trench isolation (STI) has emerged as the main road; the different approaches for STI fill and planarization will be evaluated. For the transistor integration shallow retrograde wells, sub 5 nm gate dielectrics, dual work function gates and shallow source/drain junctions are the key technologies. Logic and DRAM applications are posing different boundary conditions for integration, thus leading to different solutions for the device architecture. For high packing density memory arrays and cell based designs selfaligned contact- and local interconnect schemes has to be integrated in the frontend process flow. As a DRAM specific topic the integration challenges for trench- and stack capacitors will be addressed.

3:20pm **PS+MS-TuA5 Transient Diffusion Effects in Silicon Technology**, ***C.S. Rafferty***, Bell Laboratories, Lucent Technologies **INVITED**

In modern silicon technology, there is a steady trend to reduce the "thermal budget" of fabrication processes. The intent has been to reduce the thermal diffusion of dopants. However low temperatures have exposed significant non-equilibrium diffusion effects. The most striking of these, transient enhanced diffusion, causes many unexpected influences on devices. Transient diffusion (TED) is the enhanced diffusion rate of dopants due to point defects introduced during ion implantation. The enhancement can be as much as four decades above thermal diffusion rates. TED by its nature is cooperative in nature, where implanting one species can lead to enhanced diffusion of all the other species in the wafer, even those located some distance from the implantation window. The effects of such local and remote diffusion transients on transistors is manifold. In some cases, the transistors may fail completely to function as intended, in others, their properties may be degraded or shifted from their intended targets. This

talk describes some of the experimentally observed impacts of transient diffusion in technology. It is shown how a better understanding of the materials science involved can lead to better devices.

4:00pm **PS+MS-TuA7 Technology Requirements for Logic ICs**, ***M. Brillouët***, France Telecom, France **INVITED**

The logic ICs are targeting an higher packing density for increased performances and cost effective manufacturing. In the 'front-end' part of the process (i.e. the transistor and the lateral isolation), this higher integration is obtained - along with higher operating frequencies and reduced power consumption - in shrinking the feature sizes. As the materials stay basically the same (i.e. Si and SiO@sub 2@), this trend stresses strongly the photolithographic techniques : the etch process has to define structures at the atomic level ; selectivity, CD and profile are key parameters to control in these features with such an high aspect ratio. The density of the interconnections ('back-end' part of the process) can be improved by shrinking the feature sizes and by increasing the number of metal layers. Unfortunately, if one stays with the classical Al/SiO@sub 2@ system, while shrinking the metal pitch, the performance of the integrated circuit is degraded : there is thus a growing need to move to new materials (e.g. dual Damascene copper lines and insulators with a lower dielectric constant). Advanced developments will be required in the etching of these materials and, due to the introduction of the Damascene approach, the equipment set will be radically changed in a manufacturing line. The metallisation process impacts strongly the behaviour of the transistor : plasma induced damage during processing degrades the active devices and specific care need to be taken in order to minimize this detrimental effect. Finally, as the number of metal levels is increased, manufacturability is a major issue in the cost of the final product: improving the defectivity level of the interconnects is a key point, as more than half the process steps are now involved in the fabrication of the interconnection system.

4:40pm **PS+MS-TuA9 Advanced Deep-UV and 193 nm Optical Lithography: The Role of Resists, Reflectivity Control and Resolution Enhancement Technologies**, ***O. Nalamasu***, *R.A. Cirelli, G.P. Watson,* Bell Laboratories, Lucent Technologies **INVITED**

The fabrication of integrated circuits with optical lithography faces several challenges as the industry is moving from I-line to deep-UV and 193 nm lithographies. For the immediate future, the technical challenges in developing manufacturing processes with k values below 0.5 have been identified and are the subject of intense R&D activity across the world. The low k lithography solution requires fundamental understanding of, as well as innovations in optical and resist materials, reflectivity control and resolution enhancement (mask and optical) techniques. In this presentation, we will detail our research efforts in Resist materials, Reflectivity control and Resolution enhancement techology areas with special emphasis on 193 nm lithography and identify the issues and opportunities in extending the optical lithography for patterning sub-0.1 µm devices. We will also demonstrate 60 nm resolution with 193 nm lithography by combining research advances in single layer resist, dielectric anti-reflective layer/hard mask with a levenson phase-shifting mask.

Manufacturing Science and Technology Group
Room 317 - Session MS-WeM

Advanced Process Equipment and ES&H

Moderator: G.S. Oehrlein, State University of New York, Albany

8:20am **MS-WeM1 Complete Solvent Free Stripping of via Structures using NF@sub 3@,H@sub 2@O,O@sub 2@ Ashing Chemistry**, ***W. Au***, *R. Solis,* VLSI Technology, Inc.*; R. Bersin, H. Xu, M. Boumerzoug,* Ulvac Technologies, Inc.

The use of TiN as a base material in submicron vias employing tungsten plugs is becoming more and more accepted. One difficulty, however, is the etching of these vias and subsequent removal of polymeric residues residing at the via base and along the vertical sidewalls. Removal of these residues prior to deposition of a Ti/TiN glue layer is most critically important to achieve low contact resistance in the vias. Resist stripping and polymer-residue-removal from submicron vias is an area of intense interest at this time. Methods employing fluorine-based plasmas to render any residues DI water soluble, thereby avoiding costly and corrosive solvent processes, are under serious investigation. In this instance of TiN based vias, however, undercutting of the TiN and resulting high via resistance have been a major obstacle. A new process has been developed which address this problem. The residues are ashed utilizing a low bias RIE plasma comprising oxygen, NF@sub 3@, and H@sub 2@O vapor in correct proportions. The presence of the fluorine renders any ash residues soluble in DI water; and the H@sub 2@O vapor addition serves to inhibit the etching of the TiN base during the stripping process. The net result is a new manufacturing process which competes directly with conventional ashing and solvent processes in product performance; and which offers substantial cost savings through total elimination of solvent processing. Details of the parametric study of process conditions to achieve good TiN selectivity, excellent contact-resistance, and elimination of any TiN undercut will be discussed. A brief description of the manufacturing equipment involved will be included.

8:40am **MS-WeM2 Studies of a New High Dissociation Inductively-Coupled Plasma Downstream Strip Module**, ***W. Collison***, *T. Ni, B. Berney,* Lam Research Corp.

A new inductively-coupled high dissociation plasma downstream strip source (HD@super 2@ source) was developed to meet advanced market requirements for 200mm and 300mm photoresist stripping processes. Plasma simulations were used to study the dissociation percentage of O@sub 2@ gas for different chamber designs. It shows that this source can provide higher than 20% O@sub 2@ dissociation for 1500 watts power at 1 Torr. Fluid modeling was used to design the gas-redistribution plate to optimize ashing uniformity. Detailed process results will be presented and discussed. It is shown that adding 5-10% N@sub 2@ gas can increase photoresist etch rate 2-3 times. CHARM wafer tests have demonstrated no charging or UV damage. RF bias on the bottom electrode provides added capability to remove residues and enhance etch rate. A comparison of HD@super 2@ source and microwave source will also be discussed.

9:00am **MS-WeM3 Lithography for Smaller than 0.15 Micron Silicon Technology**, ***A. Ishitani***, Association of Super-Advanced Electronics Technologies (ASET), Japan **INVITED**

Lithography for smaller than 0.15 micron silicon technology Association of Super-advanced Electronics Technologies (ASET) Akihiko Ishitani KrF laser lithography (KrF) has reached its limits in terms of resolution capabilities, and hence it has become necessary to find practical application of such technologies as ArF laser lithography (ArF), electron beam direct writing (EBDW), and proximity X-ray lithography (X-ray) to realize further downscaling of silicon devices. As a result of research and development, these technologies have attained a resolution capability that is less than 100 nm. The remaining issues to be addressed are critical dimension and position accuracy, resist and optical materials, and mask fabrication. Defect inspection and repair technologies are important issues, too. Single layer resist technology for ArF will be employed down to 130 nm. Top-surface imaging technology for ArF, or mix and match of ArF with EBDW will be used between 150 to 70 nm, and VUV or EUV lithographies should deal with 100 to 50 nm. X-ray has enough potential for between 250 to 70 nm mass production. SCALPEL and Ion Projection Lithography (IPL) are also candidates for next generation lithography. ASET is focusing on optical lithography, X-ray, and mask writers. SCALPEL and IPL are mainly depending on the United States and Europe. In the future, lithography will be adopted to suit the type of LSI devices, depending on the required field size and the depth of focus. Mask size is another critical issue for mass production. Smaller mask size has higher capability for mask accuracy. Research and development of lithography now involve very large costs and risks, and hence international cooperation and exchange of information are essential for LSI industry. This work is being performed under the management of ASET in Ministry of International Trade and Industry (MITI) and Industrial Technology Development Organization (NEDO).

9:40am **MS-WeM5 Evaluation of Chamber Liners, in TCP Metal Etchers, to Reduce the Equipment Clean Time and to Increase the Mean Time between Cleans**, ***J. Sappidi***, *A. Liu, D. Parks, W. Au, S. Smith,* VLSI Technology, Inc.

Implementation of in-situ clean in TCP metal etchers has decreased the defect density and increased the sort yield. However, the polymer treated with in-situ clean plasma is very difficult to remove. Soaking the chamber wall with DI water or scrubbing the chamber wall to remove polymer have disadvantages. Water absorbed by chamber walls during soaking take a long time to out gas, this increases the equipment downtime. Scrubbing the chamber is very labor intensive and extends the clean time. Scrubbing combined with reactive ion bombardment during plasma processing accelerates the erosion of the chamber walls anodization. In order to reduce the clean time and increase the life of anodization on chamber walls, a set of chamber liners were evaluated. When the machine goes down for clean, rather than cleaning the entire inside chamber wall, the dirty liners can be replaced with the clean ones. This helps in reducing the cleaning time and protects the chamber anodization from eroding. . These liners were evaluated for 0.5 µm and 0.35 µm technologies. Installation of chamber liners demonstrated less than five percent process shift in terms of etchrates and selectivities. Experiments also demonstrated the metal etch process repeatability of the liner kits installation after chamber wet clean. The metal etch related defects were monitored with and without liners. The sort yield data was also collected and analyzed. The reactor with chamber liners proved superior in terms of both cleanliness and sort yield.

10:00am **MS-WeM6 Evolution Effects of Reactor Inner Wall Surface on Fluorocarbon Plasma Parameters**, *H. Oshio, M. Ogata,* ***T. Ichiki***, *Y. Horiike,* Toyo University, Japan

SiO@sub 2@ contact hole etching using fluorocarbon plasmas cause various issues such as etch stop, relating closely to the change of plasma state due to the deposition on the reactor wall. To clarify wall effects, variations of CFx(x=1-3) radical densities, pressure and wall temperatures with the C@sub 4@F@sub 8@ discharge time were investigated. Inductively coupled plasma was generated by 13.56 MHz power supplied to an antenna wound around a 130 mm @phi@ quartz bell jar connected to a 150 mm @phi@ SUS reactor. A 130 mm @phi@ Cu barrel, whose temperature was controlled by water was inserted into the reactor. An orifice head of the appearance mass spectroscope(AMS) was set at 15 cm apart from the antenna. Etching experiments were carried out on a stage equipped with a load-locked system. At first the reactor was cleaned by ashing, then pressure evolution with discharge time was measured for different residence times,@tau@. At @tau@=100 msec the pressure once dropped, and then gradually increased after 3 min. AMS revealed the pressure increase was mainly attributed to increase in CF@sub 3@ radical. The initial decrease resulted from singnificant adsorption of radicals on the cleaned wall. The run-to-run variations were measured by repeating a cycle of 3 min discharge on and 3 min off for 20 times. The wall temperature rise reached its steady state at 50 - 80 ° after the 5th run, while the pressure kept on increasing even over the 20th run. SiO@sub 2@ and Si etch rates as well as plasma potentials decreased corresponding to these increases. In contrast, at @tau@=30 msec run-to-run variation slightly occured after the 3rd run and detailed measurements of pressure evolution with time revealed no initial drop but the rapid increase after plasma ignition, caused by the high deposition rate due to the high radical density. Furthermore, water cooling of the bell jar suppressed the increase in pressures. Consequently to adopt short residence time and control the wall temperature is important for keeping CF@sub 3@ radical density constant to achieve good reproducibility.

10:40am **MS-WeM8 Studies of 300MM Poly-Silicon Etch Processes Using A Inductively Coupled Plasma Source**, ***T. Ni***, *W. Collison,* Lam Research Corp.*; K. Takeshita,* Lam Research Corp., Japan, Japan.

Inductively-coupled plasma sources have been successfully applied to 200mm poly-silicon wafer etch processes. As semiconductor wafer size increases from 200mm to 300mm, scaling up sources to meet the same or even more stringent requirements is very challenging. In this study, a

transformer coupled plasma (TCP) chamber is designed and studied for 300mm poly-silicon etch processes. Plasma simulation and Langmuir probe were used to investigate the effects of TCP power, chamber pressure, aspect ratio , and coil configuration on plasma uniformity. As a result, plasma uniformity is optimized from 5mTorr to 80mTorr. Effects of different gas injection schemes are carefully examined. It is found that gas injection has strong impact on etch uniformity and profile. A unique gas injector is designed to deliver gas efficiently and minimize profile microloading. A TCP coil is constructed to provide uniform plasma and uniform etch rate. Large conductance of the chamber allows high flow processes. Advanced control systems are implemented to improve process repeatability, minimize chamber-to-chamber variation, and increase throughput. Excellent etch results and wide process window were achieved. Detailed etch process results will be presented and discussed.

11:00am **MS-WeM9 Integrating Process Models and Operational Methods**, ***J.W. Herrmann***, *N. Chandrasekaran, R.Z. Shi, B.F. Conaghan, G.W. Rubloff,* University of Maryland

Though substantial attention is currently paid to unit process modeling/optimization and to operations/scheduling at the sector and fab levels, the relation between them has seen little exploration. This work attempts to bridge the gap between manufacturing process models and operational methods in order to systematically examine the consequences of these interactions: e.g., how the evolution of process technology will affect production, alter equipment design preferences, or suggest changes in scheduling strategies; or, what benefit to sector or factory metrics might be achieved if process or equipment improvements could be realized. The sensitivity analysis and optimization techniques in this work incorporate response surface models, which describe the manufacturing processes, and simulation and scheduling techniques, which evaluate the manufacturing system. Current work, described here, focuses on the fabrication of the tungsten plug, involving contact clean, Ti/TiN liner, and W CVD process steps carried out in a cluster tool. Response surface models for these steps are integrated in operations simulations for different cluster tool architectures (e.g., Novellus Concept II and Applied Centura) to evaluate the consequences of process-operations interactions. For each cluster tool, we describe how throughput and cycle time change as the process parameters and equipment design parameters vary. Thus, each tool's operational sensitivity is measured, which enables prediction of the impact of process changes.

11:20am **MS-WeM10 Application of an Inductively-Coupled Plasma Source to Destruction and Abatement of Fluorine-based Gases**, ***L.J. Mahoney***, *D.C. Carter, M.S. Amann, G.A. Roche,* Advanced Energy Industries

Recently high density plasma sources have been used to assist in the abatement of residual hydro-fluorocarbon and per-fluorocarbon gases which are used in many manufacturing processes. In this application, oxygen-containing gas mixtures are added with the exhaust gases from a vacuum process chamber within the foreline of a processing system. The mixture is then activated by a high-density plasma means in order to converted the hydro-fluorocarbon and per-fluorocarbon process gases into constituents that are more easily removed from the exhaust within an air scrubber. An economical and modular inductively-coupled plasma source has been devised to investigate the power coupling and process requirements necessary to effectively abate post-process gases by this method. The relatively high power density source is configurable to operate near 400 kHz , 2 MHz or at 13.56 MHz with more than 2 kW of delivered power. Abatement destruction efficiencies are shown for several gases including CF@sub 4@, C@sub 2@F@sub 6@, CHF@sub 3@, and SF@sub 6@ as determined by mass spectroscopy over a wide range of power, pressure, and total flow conditions and range of added oxygen/argon/nitrogen gas mixtures.

11:40am **MS-WeM11 Low Dielectric Polymer Etching with a Downstream Microwave Plasma**, ***R.R.A. Callahan***, *G.B. Raupp, S.P. Beaudoin,* Arizona State University

The semiconductor industry has signed a memorandum of understanding with the EPA to reduce the amount of fluorocarbon gases used. In particular, this impacts the way that silicon dioxide etching is performed. At the same time, new dielectric materials that offer lower dielectric constants than silicon dioxide are required to help reduce chip speeds. Polymer dielectrics offer reduced dielectric constants compared to silicon dioxide, and they also can be etched using oxygen, not fluorocarbon gases. We have studied the etching of parylene films using a downstream microwave oxygen plasma, and we will report on the effects of temperature on the etch rate and will provide a tentative etching mechanism.

Manufacturing Science and Technology Group
Room 317 - Session MS-WeA

Process Control and Yield from Tool to Factory

Moderator: S. Shankar, Intel Corporation

2:00pm **MS-WeA1 Factory Implementation of Process Control: Technical or Cultural Challenge?*, K.G. Vickers,*** Texas Instruments **INVITED**

The use of systematic, company wide process control techniques in integrated circuit manufacturing factories (known as wafer fabs) have been low since the inception of the industry in the 1960s. Reasons for this low implementation of process control methods have included both technical and cultural barriers to implementation. The technical barriers that have hampered process control implementation in wafer fabs originated from both the unique nature of IC fabrication processing and the rapidly changing equipment sets needed to build ever advanced technology node integrated circuits. These technical barriers included the simultaneous continuous flow and discrete event nature of most processes, the high number of equipment types/processes in an IC product flow, the significant changes in required process output from run to run, and the lack of computing power to handle a large diversified data stream. In recent years these technical barriers been reduced to the point that the size of the cultural barriers have become obvious as the major obstacle to successful systematic implementation. These cultural barriers originated in early wafer fabs whose technical population was strongly focused on device characteristics rather than process stability, whose reward and recognition system was based on local problem solutions rather than systematic solutions, and whose manufacturing methods were created locally rather than through company wide standardization. Over the last fifteen years Texas Instruments has achieved some success in overcoming first the technical barriers and then the cultural barriers for systematic implementation of advanced process control techniques in all TI world wide wafer fabs. This presentation will highlight the necessary technical changes that were put in place, and a key set of cultural changes that were implemented, to gain the benefits of systematic process control in a world wide manufacturing environment.

2:40pm **MS-WeA3 Advanced Process Control and Sensor Requirements for Reducing Non-Product Wafer Usage and to Increase Tool OEE in 300mm Manufacturing*, M.L. Passow,*** *J. Pace,* IBM Corporation **INVITED**

To maintain productivity in leading edge manufacturing, shrinking feature sizes and increases in equipment productivity are necessary. The shift from 200mm diameter wafers to 300mm diameter wafers is required, but not sufficient. Improvements in equipment OEE and reductions in the usage of non-product (NP) wafers and SAHD wafers must be made as the cost of using conventional methods of control in new, fully automated 300mm fabs is too high. Based on learning gained by understanding NP wafer usage in 200mm development and manufacturing lines, areas with the highest potential benefit from various reduction strategies will be identified. Process tool suppliers will be requested to incorporate Advanced Process Control (APC) strategies where possible. Adherence to standards will be required to facilitate the adaptation of new sensor, APC, data collection, and line management strategies to meet these needs. Particular recommendations will be presented.

3:20pm **MS-WeA5 Process Module Control Technology for 300mm Plasma Processing*, F. Kaveh,*** *B. McMillin, W. Collison,* Lam Research Corporation **INVITED**

In order to meet the challenge posed by the processing of the 300mm wafers, and the move toward sub quarter micron feature sizes, a new hybrid etch tool control architecture has been devised. This new architecture, based on TI's ControlWORKS environment, has enabled close coupling of a number of feedback loops for control of equipment level parameters, as well as control of stand alone remote sub-systems. Through the use of VME based direct I/O, for fast loops, and LonWorks network for less time critical loops, effective partitioning and optimization of the control functions has been achieved . Through the digitization and integration of a number of the process control loops such as the match and pressure controllers, measurable improvements in the overall operation of the tool has been realized. Further, a structure has been put in place that allows further integration of the aforementioned loops, and implementation of outer loops, for plasma state control applications. The new architecture is highly flexible, and as such, has enabled the integration of various sensors, such as an optical emission spectrometer, and a low cost RGA. These sensors are being used for detailed characterization of the chamber and the plasma, and are expected to result in significant gains in tool productivity and performance.

4:00pm **MS-WeA7 Using Wafermap Data for Automated Yield Analysis@footnote 1@*, K.W. Tobin,*** *T.P. Karnowski, S.S. Gleason,* Oak Ridge National Laboratory*; D. Jensen, F. Lakhani, C. Long,* SEMATECH **INVITED**

To be productive and profitable in a modern semiconductor fabrication environment, it is required that large amounts of manufacturing data be collected and maintained. This includes data collected from in-line and off-line wafer inspection systems and from the process equipment itself. This data is increasingly being relied upon to design new processes, control and maintain tools, and to provide the information needed for rapid yield learning and prediction. Because of increasing device complexity, the amount of data being generated is outstripping the yield engineer's ability to effectively monitor and correct unexpected trends and excursions. The 1997 SIA National Technology Roadmap for Semiconductors highlights a need to address these issues through "automated data reduction algorithms to source defects from multiple data sources and to reduce defect sourcing time." In this paper, we will discuss the current state of yield management automation and the role that SEMATECH and the Oak Ridge National Laboratory@footnote 2@ are taking in directing and developing new technologies that will provide the yield engineer with higher levels of automated data reduction and analysis. Yield management systems have been evolving over the past decade from a primary role of database storage and retrieval to systems that provide timely insight into the current state of manufacturing. The evolutionary process can be described in terms of five fundamental steps: (1) infrastructure and database management; (2) processes that add context to the data, i.e., that add information; (3) the use of data and context to find patterns, i.e., extract information; (4) methods of interpreting patterns, i.e., extracting knowledge; (5) and the automated application of process knowledge to yield management. In this paper we will focus on step (2), technologies which add context to data. In particular, we will discuss ORNL's contributions to the fields of automatic defect classification (ADC) and whole-wafer spatial signature analysis (SSA) for optical and electrical test data. We will also discuss preliminary results in the field of manufacturing-specific, content-based image retrieval (MSCBIR). MSCBIR is an image-based datamining technology that allows engineers to search a large image repository using an image of a semiconductor defect event as a query to locate other images that are similar in appearance. This exciting new technology is valuable due to the highly image-oriented approach taken by the yield engineer in problem solving, and the vast quantities of images stored in yield-management databases (approximately 70% of the total data). The ability to automatically extract content from raw manufacturing data will be a key factor for automating the discovery of knowledge in the dynamic semiconductor manufacturing environment. The current state of the art in yield management is only now beginning to comprehend these capabilities. Potential future applications of this knowledge in areas such as auto-sourcing statistical process control, condition-based maintenance of process tools, and yield prediction will also be briefly presented. @FootnoteText@ @footnote 1@K.W.T. (Correspondence): E-mail tobinkwjr@ornl.gov; WWW: http://www-ismv.ic.ornl.gov; Telephone: (423) 574-8521; Fax: (423) 574-6663. @footnote 2@Work Performed for SEMATECH, Austin Texas, under Contract No. ERD-95-1340 and prepared by OAK RIDGE NATIONAL LABORATORY, Oak Ridge, Tennessee, 37831-6285, managed by LOCKHEED MARTIN ENERGY RESARCH CORP. for the U.S. DEPARTMENT OF ENERGY under contract DE-AC05-96OR22464. @footnote 3@ K.W. Tobin, S.S. Gleason, F. Lakhani, and M.H. Bennett, "Automated Analysis for Rapid Defect Sourcing and Yield Learning", Future Fab International, Issue 4, Vol. 1, Technology Publishing Ltd., London 1997, p. 313.

4:40pm **MS-WeA9 Visual Data Mining of Defectivity Data using Parallel Coordinates*, A. Chatterjee,*** IBM Research **INVITED**

Defectivity data from a 4MB DRAM manufacturing process was analyzed using a visual data mining methodology based on Parallel Coordinates. Parallel Coordinates provides an interactive framework for analyzing multi-variate data graphically using 2-D graphs that can be colored using visual queries. These graphs provide a unique mapping of multivariate data to 2-D without any loss of information. Using this methodology, some defects were found that were actually "beneficial" and in small quantities improved the yield and speed performance (access time) of the wafer. While using conventional methods, the yield on the wafers couldn't be improved beyond a plateau and hence had led the engineers to think of redisgning

the chip, the process window discovered using the Parallel Coordinate methodology provided some insights that helped in improving the yield of the process significantly. This technique is extremely useful in yield analysis and improvement, process control and design of experiments.

Manufacturing Science and Technology Group
Room 317 - Session MS-ThM

Sensors and Support Technology
Moderator: B. Van Eck, SEMATECH

9:00am **MS-ThM3 RF Monitoring of PECVD Tools in a Manufacturing Environment**, ***M.B. Freiler,*** IBM

The use of RF monitoring systems for plasma enhanced chemical vapor deposition (PECVD) tools in an advanced microelectronics production environment is discussed. Data obtained from the measurement of RF current and voltage at the input to the process chamber provides valuable process information that is unavailable from data recorded using traditional process control techniques, such as RF forward and reflected power. RF current and voltage data is presented for silicon oxide and nitride films deposited in commercial PECVD reactors. The application of this data to improvement of the periodic chamber cleaning process with the goal of reducing gas emissions and chamber contamination will be shown. In - film wafer contamination measurements showed an improvement of 10 X in number of particles when the improved clean was implemented. RF measurements have also been used to improve the effectiveness of post - clean chamber seasoning, by giving an indication of the completion of the seasoning. Inadequate seasoning will result in increased variability of film thickness and stress. Changes in RF current and voltage during the deposition process give an indication of this increase in variability. Finally, the application of RF measurements to reactor matching will be discussed; RF signal strength of different reactors running the same process can be compared in order to understand and control performance differences between the reactors.

9:20am **MS-ThM4 Advances in Broadband RF Sensing for Real-time Control of Plasma-Based Semiconductor Processing**, ***C. Garvin,*** *D.S. Grimard, J.W. Grizzle,* The University of Michigan

Ever shrinking geometries are putting heavy pressure on sensor systems to provide adequate process knowledge for control and diagnostics. Plasma processing specialists in industry and academia have recognized that a substantial amount of information about the plasma state should be contained in the RF signal (13.56 MHz) and its harmonics. On the surface, making measurements for control purposes should be straightforward, and the real work should lie in making the connections (mathematical models) between measurements and key plasma quantities. Unfortunately, this is not the case. Work reported in this area from major University and Government research facilities, as well both US and Japanese chip manufacturers, has shown disappointing results and revealed that the RF sensing problem itself is non-trivial. An approach which has shown promise is `broadband sensing', a novel sening method based on the Resonance Probe used in ionospheric physics. The goal of the broad band RF work is to create a diagnostic with much greater signal to noise ratio, and much higher sensitivity to the plasma state and its environment than standard RF sensing. The idea is to scan the plasma with a very low wattage, broad band RF signal from 100 MHz to 1 GHz, measuring the reflected signal. In a typical scan, the large amount of data taken over a wide range of frequencies provides redundancy and enhances the signal to noise ratio of the sensor. Preliminary work has shown this sensor to have favorable performance when compared to standard RF sensing. We will present novel results of a non-intrusive implementation of the sensor.

9:40am **MS-ThM5 NOVA In-Line CMP Metrology and Its Use for Lot-to-Lot Process Control**, ***T.H. Smith,*** Massachusetts Institute of Technology*; S.J. Fang, J.A. Stefani, G.B. Shinn,* Texas Instruments*; D. Boning,* Massachusetts Institute of Technology*; S.W. Butler,* Texas Instruments

The use of in-line metrology with run by run (RbR) process control is becoming a means to meet the future demands on improved processing quality without sacrificing throughput. This control will become critical for large variation processes such as chemicalmechanical polishing (CMP). In response to this, other works have described the use of the NOVA in-line CMP metrology system for use in RbR process control. This work describes a similar system, but focuses on quantifying 1) the quality of measurements obtained from the NOVA system, 2) improvements gained by simple RbR control of post-polish patterned wafer thickness over fixed-time polishing and pilot wafer control, and 3) the increases in throughput using an in-line measurement and control system. The results of a gauge study of the NOVA system and a 600 wafer RbR control experiment performed at Texas Instruments, Inc. are discussed. The variability of the system is shown to be well within standard requirements. The reliability of the system over the 600 wafer experiment was very good. The NOVA measurements are shown to correlate well with ex-situ measurements. The 600 wafer RbR control experiment indicates that even a simple control approach provides a 25% improvement over the fixed-time approach. The results demonstrate that controlling directly on patterned wafers provides a 23% improvement over control using pilot wafers. The experiment shows a 25-40% improvement in throughput using the system. The number of cleans were reduced by 0-66% (depending the number of look-aheads and amount of re-work) and ex-situ measurements were eliminated, indicating significant cost of ownership reductions.

10:00am **MS-ThM6 In Situ CD Measurement during Post Exposure Bake**, ***R.H. Krukar,*** Bio-Rad Semiconductor*; N.T. Sullivan,* Digital Semiconductor*; S.L. Prins, J.R. McNeil,* Bio-Rad Semiconductor

As critical dimensions are reduced below 0.18 micron, post exposure bake is emerging as a critical and controllable process. Direct correlations between bake times and line width have been reported. We built an in-situ post exposure bake sensor and monitored the critical dimensions of a SRAM pattern as it baked. The data indicates that production of an accurate in-situ PEB monitor is possible.

10:20am **MS-ThM7 Process Environment Monitoring of Plasma Etching for Advanced Process Control**, ***H. Enami,*** *A. Kagoshima,* Hitachi, Ltd., Japan **INVITED**

The development of 0.18um process is our current target. Some equipment, at present, cannot meet the requirements from the process (e.g. Selectivity, uniformity, aspect ratio, etc., in dry etching). Considering the facts: (1) Physical limitation against the countermeasures in equipment (2) Decrease of Overall Equipment Effectiveness due to increasing QC time, we suggest quick installation of advanced process control (APC) system such as In-Situ control. To make the best use of In-Situ Control, following 3 steps are necessary. (1) To find useful methods and instruments for process condition analysis. (2) To make digital network among instruments for analysis and to reduce sampling period (less than 1 sec./time) and the prices of those instruments. (3) To find a correlation between monitoring data and process condition or results. Firstly, In-Situ data comparison between Plasma Probe Data and RF Impedance (RFIM) Data shows that RFIM is more useful monitoring method than Plasma Probe for unstable plasma discharge and fluctuating process condition. Secondly, Plasma diagnostics by Plasma Optical Emission Spectroscopy (OES) per sub-micro-sec shows that Pulsed-Plasma-Discharge contributes to improve etching uniformity and control the quantity of etchant. Quadrupole Mass Spectrometry (QMS) is also useful for the same purpose. Comparing OES and QMS, OES is useful for short life species in plasma, on the other hand OMS is for reacted species or products. Both are necessary as In-Situ-Monitoring. In dry etching (SiO@sub 2@ film) process, for example, the combination of OES and RFIM for Gas flow rate and RF Power control contributes to reduce the dispersion of Selectivity among wafer to wafer in a batch to 25% of it without control. This data shows the advantage of In-Situ Control by simple, convenient and high-speed sensor. Then we have began the development of process control system using RFIM, OMS, OES allowing more than one time feedback per second.

11:00am **MS-ThM9 Improvement of Process and Equipment Performance Using Online and Real Time Optical Emission Spectroscopy**, ***D. Knobloch,*** Siemens Microelectronics Center GmbH & Co. OHG, Germany*; F.H. Bell,* Siemens AG, Germany*; J. Zimpel,* Fraunhofer Institute, Germany*; A. Steinbach,* Siemens Microelectronics Center GmbH & Co. OHG, Germany

The semiconductor industry is continually driven towards the use of larger wafers (200 mm and larger) and smaller device dimensions (0.18 mm). More and more sophisticated technologies are necessary to improve overall production performance and reduce manufacturing costs. Intelligent process and equipment control applied to plasma processing is an excellent candidate to improve productivity, and thus profitability. We use optical emission spectroscopy to characterise etching processes for 64Mbit DRAM fabrication by in-situ analysis of plasma conditions. Parameters to be optimised include: increased wafer throughput and wafer yield, reliable processes, reduction of monitor wafers, optimisation of cleaning procedures. Four MxP@super +@ oxide etch chambers mounted on a Centura platform are equipped with optical multichannel analysers (200 - 950nm). The dynamic evolution of the spectra can be recorded every 20msec during wafer processing. The spectrometers are coupled to the etch chambers via the fab host computer allowing in-situ and real time process and equipment control. Intelligent data reduction techniques, such as principal component analysis (PCA), are used to extract process and

equipment related wavelength ranges. Every process parameter, such as pressure, power and gas flows, shows a typical optical signature. Therefore, the cause of process variations can be determined. Furthermore, even without variation in the external parameters, the plasma processes are plagued by process drift phenomena: the process performance (e.g. etch rate, uniformity, selectivity) varies continually as a function of time. These phenomena are linked to the chemistry occuring at the reactor walls and the influence of thin films deposited by the plasma. These drifts can be correlated to changes of certain wavelength ranges in the optical emission spectra. Major benefits of this technique are early process fault detection and optimisation of chamber cleaning cycles. @FootnoteText@ The presented work was part of a project funded by the saxonian department of economy (SMWA), project number: PT2648.

11:20am **MS-ThM10 Multivariate Spectral Analysis of Optical Emission Spectroscopy for use in Low-Open Area Endpoint Detection**, *D. White,* ***B. Goodlin****, A. Gower, D. Boning, H. Sawin,* Massachusetts Institute of Technology*; T. Dalton,* Digital Equipment Corporation

As device dimensions continue to shrink, the need for tighter control of semiconductor processes is increasing. In particular, accurate determination of endpoint in plasma etching processes is essential to decrease defects due to both incomplete clearing of the etched material and excessive overetch of the underlying material, leading to a loss of dimension control. This is particularly challenging for low open area etches (<1%), where traditional sensors are at the limits of their sensitivities in determining endpoint. Many sensors have been utilized for the purposes of determining endpoint including optical emission spectroscopy(OES), laser interferometry, optical emission interferometry, mass spectrometry, and rf impedance monitoring, but OES is the most widely used sensor. Traditional endpoint algorithms using OES observe only a few selected wavelengths corresponding to major product and reactant species, thus utilizing only a small fraction of the data provided by OES. For instance in an oxide etch process, using C@sub 2@F@sub 6@, we might follow the emission lines corresponding to a reactant species C@sub 2@ (e.g. 516 nm) and a product species SiF (e.g. 440 nm) during an etch process. Endpoint would be indicated by an increase in the ratio of the C@sub 2@ line intensity to the SiF line intensity. Since both lines are changing in intensity at endpoint we say that these lines are correlated or covarying. The OES spectrum, however, consists of a number of other emission lines which also correspond to reactant and product species, including many more lines corresponding to the many different excitations of C@sub 2@ and SiF. All of these lines have correlated changes that occur at endpoint, so by throwing away all of the spectra except a few spectral lines, the traditional endpointing algorithms do not take full advantage of all of the information available, resulting in a lower signal to noise ratio than that resulting if all of the lines were kept. In this paper, we examine the use of a multivariate technique called principal component analysis (PCA) which utilizes the entire OES spectrum and thus demonstrates superior signal to noise over the traditional univariate methods. We then demonstrate the technique for real-time endpoint detection in an industrial oxide contact etching process with low open areas (~1%). Lastly, implementation issues such as adjusting for process drift due to window fogging and PCA model validation are discussed.

11:40am **MS-ThM11 Simulations of the Performance of Novel Ion Current Sensors**, ***M.A. Sobolewski,*** National Institute of Standards and Technology

To obtain optimal results from plasma processing, the properties of ions and neutrals incident on the substrate must be carefully controlled. If sensors for the relevant properties of the ions and neutrals were available, they could be used to detect process drift and equipment malfunctions, diagnose their origin, and take correction action, if needed. One particularly important parameter to monitor is the total ion current at the substrate. Recently, a method has been demonstrated for using external, radio-frequency (rf) electrical measurements to monitor the ion current at an electrically insulating or conducting wafer during processing by a high-density plasma.@footnote 1@ The rf signals are generated by the rf bias power which is normally applied to wafers. There is no need for any probe to be inserted into the reactor or for any additional power supplies which might perturb the plasma. At low rf bias frequencies (0.1-1 MHz) ion currents measured by this technique agree well with dc measurements of the ion current, but they agree less well at higher frequencies.@footnote 1@ In this work, this disagreement was investigated using a fluid model of the sheath region of high-density plasmas. Simulations show that, as the rf frequency approaches the ion plasma frequency at the edge of the sheath, the ion current at the electrode varies strongly with time during each rf period. Under these conditions, the rf measurement of ion current differs from the time-averaged value of the ion current. The simulations are used to characterize the error in the rf measurement technique and to suggest new rf methods which more accurately determine the time-averaged ion current. @FootnoteText@ @footnote 1@M. A. Sobolewski, Appl. Phys. Lett. 72, 1146 (1998).

Partial Pressure Measurements and Process Control Topical Conference
Room 317 - Session PC-ThA

RGA Characteristics and Calibration

Moderator: S.A. Tison, Millipore Corporation

2:00pm **PC-ThA1 Semiconductor Applications of a Quadrupole Mass Spectrometer**, ***R.K. Waits,*** MKS Instruments **INVITED**

Commercial quadrupole mass spectrometers (QMSs) became available in the late 1960s and have been popular in R&D labs, but until recently have found limited use in semiconductor manufacturing. To sample at pressures above 10@super -5@ Torr with ppm sensitivity or better (relative to the total process pressure), differential pumping is usually required. The newly-available, small, high-pressure QMS sensors can operate as high as 10 to 20 mTorr without differential pumping, but provide somewhat lower mass resolution and partial pressure sensitivity than a standard QMS. Applications in the semiconductor fab include equipment monitoring, process monitoring and effluent analysis. Equipment monitoring can include qualification after preventative maintenance, rate-of-rise tests, and leak identification and detection. Usually the burning question is: Why won't the vacuum chamber pump down? Other uses that are not usually considered include the qualification of replaceable parts: sputter cathodes, electrodes, lamps, shields, etc. The trend to smaller features and thinner layers on larger, more expensive wafers requires better in-situ monitoring of fabrication processes. In process monitoring, the key question is: Is this process running normally? A manufacturing monitor can be useful simply by providing a comparison between a well-behaved high-yield process and a marginal or failing process. Experience mixed with a little process expertise can link the symptoms, as shown by QMS spectra, with the root cause of the disease, result in a prompt cure, and lead to continuous process improvement. Examples will be given for physical vapor deposition (sputtering) processes, chemical vapor deposition and plasma etching. The effluent from chemical vapor deposition and plasma etch processes can be analyzed to measure the efficiency of process gas utilization or to monitor the efficacy of abatement methods used for the removal of global warming gases.

2:40pm **PC-ThA3 In Situ Monitoring of Semiconductor Reactive Gas Processes using Partial Pressure Analyzers**, ***L.C. Frees,*** Leybold Inficon, Inc. **INVITED**

As semiconductor fabrication is pushed towards narrower linewidths utilizing new materials, processes such as chemical vapor deposition (CVD) and etch increasingly employ reactive gases. These gases, along with high temperatures and/or plasmas, and process pressures ranging over six orders of magnitude (1E-1 to 1E+5 Pa) present considerable challenges to the partial pressure analyzers (PPAs) and systems used to monitor them. Techniques used in the design and construction of the sample inlet system, the differential pumping system and the PPA itself which result in a viable in situ process monitor will be discussed. Emphasis will be given to the ion source itself. Choices concerning the place on the process tool to connect the PPA, and their effects on the data obtained, will also be covered. Applications examples will include CVD of the metals Cu, Ti (and TiN), and W and Al. Also included will be the CVD of dielectrics such as silicon nitride and phosphosilicate glass. Sampling methods for monitor etch processes for both metals and dielectrics will be presented, with a focus on the lifetime of the ion source.

3:20pm **PC-ThA5 Emission Free Measurement of Residual Gas in XHV Using Ionization by Trapped Electrons in Magnetic Field**, ***A. Yamamoto,*** *S. Kato,* KEK, Japan

One problem associated with partial pressure measurement in an extremely high vacuum (XHV) region is outgassing from an ion source of a residual gas analyzer (RGA) itself. In order to reduce the outgassing, an improvement of its structural materials of the ion source was reported previously.@footnote 1@ However there still remains a problem of thermal outgassing from the ion source as far as a hot filament is used. Therefore, it is required for suppressing thermal outgassing to limit a time of electron emission from a filament. In this work we used a hot filament for a limited time in the beginning of the measurement. Adopting an axial magnetic field to a cylindrical anode to make a flight time of emitted electrons long, we could keep electrons trapped inside. These trapped electrons allowed us to ionize the residual gas without the thermal outgassing. But dwindling of the number of electrons due to the electron - gas collisions leads to decreasing of ion currents. We measured a dependence of the decay of ion currents for He, Ne, N2 and Xe on a gas pressure in a range of 10@super -7@ to 10@super -8@ Pa. And we also compared the decay of ion currents for the different gas species in the same pressure range. We verified that the decay time decreased with an increase of the pressures or the molecular diameters. @FootnoteText@ @footnote 1@S.Watanabe, M.Aono, S.Kato, J. Vac. Sci. Technol. A 14, 3261 (1996).

3:40pm **PC-ThA6 Residual Gas Analyzer Ion Current Measurement, Calibration and Partial Pressure Detection Limits**, ***R.E. Ellefson,*** *A.J. Kubis, L.C. Frees,* Leybold Inficon, Inc.

Ion detection in a residual gas analyzer (RGA) is by faraday detector with electrometer and/or a secondary electron multiplier detector that use the same or separate electrometer. The minimum detectable partial pressure (MDPP) measured by these detectors is a ratio of noise(A) of the detection system to the sensitivity(A/Torr) of the RGA for each detector type. Critical to the statement of MDPP is the inclusion of the integration (dwell) time interval used to determine the noise value. Usually the MDPP reported is the longest integration time period of the RGA which produces the lowest number. However, the user normally uses integration times of the order of 0.25 s or less to rapidly get data for timely observation of the process. In this paper we present a model for predicting MDPP as a function of integration times from 8 ms to 4 s based on detector noise and ion statistics. Separately we present ion current measurements of the @super 36@Ar and @super 38@Ar minor isotopes of argon as a function of pressure to demonstrate practical detection limits of a RGA as a function of integration time. Additionally, we present data from the systematic dilution of standard gas mixtures and from a fixed composition flow standard that validate the low ppm detection limits for impurities in Ar.

4:00pm **PC-ThA7 Practical Quadrupole Theory: RGA Characteristics**, ***R.E. Pedder,*** ABB Extrel **INVITED**

Residual Gas Analyzers (RGA's) are commonly used to monitor the partial pressures of contaminants, process gases and reaction gases in various vacuum processes. Quadrupole mass filters can be used as RGA's through the application of RF and DC voltages in such a way as to make ions of a single mass or narrow range of masses to transmit through the quadrupole to the detector. The physics that describes the trajectories of these ions through this electrodynamic field is well studied. The performance characteristics that can be inferred from such trajectories have been predicted through both analytical and numerical methods. Unfortunately, the mathematics involved, while straightforward, is often beyond the comfort level of the practical experimentalist. This presentation will include a broad review of practical quadrupole theory, utilizing graphical means to illustrate the indicators to quadrupole performance, and avoiding all but the most straightforward equations. The goal of this presentation is to provide a more intuitive understanding of quadrupole operation, with emphasis on practical issues. Key performance figures of merit will be identified along with a practical analysis of the theoretical indicators to performance (e.g. transmission/sensitivity is proportional to the square of the rod diameter, resolution and abundance sensitivity increase with increasing RF frequency). Performance characteristics of a wide spectrum of analyzers will be compared. The performance compromises that are inherent in the optimization of quadrupole analyzer characteristics for a given application will be reviewed.

4:40pm **PC-ThA9 Residual Gas Analyzer Performance Characteristics**, ***C.R. Tilford,*** National Institute of Standards and Technology*; T. Gougousi,* University of Maryland

Reliable process monitoring and control require reliable instrumentation. Residual gas analyzers (RGAs) are promising candidates for these applications, but only if they are properly adjusted and used. The National Institute of Standards and Technology's (NIST) earlier work on the performance characterization and calibration of conventional, or open-source RGAs, is being extended in collaboration with the University of Maryland. This new work includes the characterization of closed-source RGAs, the development of in situ RGA calibration techniques for use in a CVD tungsten deposition tool, and the application of the calibrated RGAs in the monitoring and control of the tungsten deposition process. This talk describes fundamental characteristics of RGAs that limit their performance, and techniques to detect and minimize these undesirable characteristics. Particular attention is paid to operating conditions that cause the sensitivity for one gas to depend on the pressures of other gases.

5:00pm **PC-ThA10 Calibration of Gas-Analytic Mass Spectrometers for Gases and Vapors**, ***R. Dobrozemsky***, *G.W. Schwarzinger,* Vienna University of Technology, Austria

The demand to quantify pressure-, density-, and flow-rate-readings is steadily growing, e.g. for quality control. By many reasons, simple and reliable in-situ calibration methods for pressure-reading instruments (e.g. BA-gauges) and partial pressure analyzers (e.g. quadrupole mass spectrometers) are required. In this contribution, the potential of in-situ methods for calibration of vacuum instruments is discussed, with special attention on admitting gas bursts, defined by expansion of known quantities of gases and vapors. Ten years ago, a "gas-burst calibration" procedure for non-reactive gases has been introduced at Seibersdorf.@footnote 1@ Recent demands in geological research and space technology led to new calibration procedures for water- and oil-vapors (thermal decomposition method - TDM and crack-product calibration - CPC, respectively). By these methods, in-situ calibrations can be done with an accuracy of 1 to 3% for non-reactive gases (e.g. H@sub 2@, N@sub 2@, CO, CO@sub 2@, CH@sub 4@, He, Ar, etc.), of about 10% for water vapor and of about 20 to 40% for oil vapors. Moreover, calibrations can be repeated several times a day, if necessary (e.g. under harsh conditions), and ca be performed in a wide pressure range down to uhv. @FootnoteText@ @footnote 1@ R. Dobrozemsky, Vacuum 41, 2109 (1990)

Manufacturing Science and Technology Group
Room Hall A - Session MS-ThP

Manufacturing Science and Technology Group Poster Session

MS-ThP1 Dynamic Simulation Based Learning Tools for Manufacturing Education and Training, ***G.W. Rubloff***, *A.R. Rose, Y. Sankholkar,* University of Maryland*; D.E. Eckard,* North Carolina State University

A critical issue for the semiconductor manufacturing industry is the skill of the workforce at all technical job levels. The challenge of education and training is especially difficult because it is highly labor intensive and because the reality of actual hardware is very expensive and difficult to access for training purposes. We have constructed software learning tools as an avenue to dealing with both problems. They exploit physically-based dynamic simulation, so that the learner may "operate" sophisticated equipment, even break it, without adverse consequence but with the opportunity to understand how the equipment and process work. The simulators are accompanied by integrated tutorial, guidance, and reference material to support the learner in exploring phenomena, principles, and physical behavior of the system. As self-contained learning tools, disseminated as software or across the Internet, these learning modules provide the opportunity to learn when and where the student chooses. The software platform is constructed to relate guidance materials directly to simulator objects, to support experimentation and record-keeping, to permit learner-directed exploration in depth, through examples, and through exercises and self-tests, and to facilitate authoring of tutorial material and construction of physically-motivated simulators and error handling with minimal need for manufacturing practicioners to write software. Learning modules are demonstrated which convey vacuum and gas flow, heat transfer, chemical reaction, and other concepts and realizations relevant to semiconductor manufacturing equipment and process.

MS-ThP2 Surface Cleaning on Aluminum for UHV using Supercritical Fluid CO@sub 2@ including NaCl and H@sub 2@O as Impurities, ***T. Momose***, *H. Yoshida,* Miyagi National College of Technology, Japan*; Z. Sherverni, T. Ebina, Y. Ikushima,* National Industrial Research Institute of Tohoku, Japan

Ozone treatment has been applied to several metals for UHV to improve outgassing rate. The surface of the ozone treated Al and superconducting Nb cavity @footnote 1@ showed the low adsorption characteristics and low density of hydroxide in the surface. These suggest that removal of the native oxide and the treatment without water can improve vacuum characteristics of the surface. Conventional surface treatments cause inhomogeneity and need water cleaning process. Therefore, we investigated the treatment with supercritical CO@sub 2@ because supercritical CO@sub 2@ can readily dissolve nonpolar compounds. Before the removal of surface oxide and ozone treatment, supercritical CO@sub 2@ was applied to the UHV material such as Al to clean the surface. A sample was a half piece of a swagelok cylinder (10.8 mm in diameter and 8.5 mm in length) cut along the axis with hard almite coating. CO@sub 2@ was supplied from a tank and charged into a syringe pump (HPB-350) via a cooler at about -10 °C. Liquefied CO@sub 2@ was transferred into a high pressure chamber made of stainless steel 316 cylinder with inner diameter of 50 mm, inner length of 50 mm and thickness of 20 mm. The surface analysis was carried out by XPS. The cleaned level was evaluated by the density (at%) of carbon (C) determined from the ratio of convoluted area of Al2p, O1s, and C1s peaks. The C density of untreated Al was 87 %. The C density of Al treated by supercritical CO@sub 2@ at 70 °C and 94 atm for 2 hours was 65 %. Furthermore, the C density of the surface treated by the addition of H@sub 2@O of 0.5 cc and NaCl of 0.05 g to supercritical CO@sub 2@ at 100 °C and 150 atm for 2 hours decreased to 13 %. The treatment with the same fluid showed no C density (13-25 %) dependence on pressure ranging from 100 to 250 atm. The treatment also showed the black surface which was locally oxidized with the aid of the contact potential with the chamber. Similar results were observed on the almite coating of the sample. @FootnoteText@ @Footnote 1@T. Momose. et. al., Vacuum, 47, No4, 319-324.

MS-ThP3 Design of Dynamic Simulation Experiments for Assessing Manufacturing Metrics, ***R.Z. Shi***, *Z. Han, K. Moores, E. Li, Z. Chen, G.W. Rubloff,* University of Maryland

Evaluation of equipment and processes commonly focuses on raw process time, with equipment overhead contributions to cycle time playing a secondary and/or separate role in decision-making. This work is directed at equipment and process design while treating on an equal footing the contributions to cycle time which arise from raw process time and the cycle time elements associated with establishing process conditions and recovering from them after process completion. Design of experiments (DOE) methodology (using commercial ECHIP@super TM@ software) and dynamic simulation (using a previously designed simulator based on VisSim@super TM@ software) are employed to optimize a rapid thermal CVD polySi process. The RTCVD simulator captures the essential physics and chemistry of mass transport, heat transfer, and chemical kinetics of the RTCVD process as embodied in a specific equipment design. Various parameters for process recipe as well as for equipment design were first selected as possible factors for the response deposition rate and cycle time. A screening design was first carried out to choose those most significant factors, followed by more extensive experiments leading to the generation of response surface models, i.e., for deposition rate and cycle time. The results reveal different regimes of process and equipment design in which cycle time is primarily determined by raw process time, as well as regimes where equipment design is critical in its influence on overhead contributions to the total cycle time, e.g., for establishing reactor pressure initially, or for wafer cooldown. This work demonstrates that the combination of DOE methodology and dynamic simulation provides a powerful tool for examination and optimization of multiple figures of merit; these include more complex but critical metrics like the full cycle time, as well as more specific process measures such as steady-state deposition rates.

MS-ThP4 Fluid Simulation of Distributed Gas Injection for Aluminum and Photoresist Etch, ***D.F. Beale***, *N. Williams,* Lam Research Corporation

The differences between two gas injection designs were studied via 3D fluid simulations. The two cases considered were a typical showerhead injected reactor with side pumping and a novel distributed injection reactor. In the novel design, gas entered the reaction chamber subsonically through a hexagonal array of cells. Each cell consisted of a circular gas inlet port with a concentric annular outlet port. Simulations of both designs were performed for a typical low pressure Aluminum etch and a high pressure photoresist (PR) strip. Plasma effects were not considered because the commercial fluid simulation used predicts Al etch trends well@footnote 1@ and because the stripper plasma was distant from the wafer. Peclet number values calculated from simulation output showed more diffusive transport in the novel geometry than in the standard one. This difference was important for the transport-limited etching of Al by Cl@sub 2@, but not for the interface-limited etching of PR by O@sub 2@. Differences between the two etch chemistries were further characterized via Reynolds numbers, Knudsen numbers and sticking coefficients calculated from simulation output. Axisymmetric 2D simulations of a showerhead-injected reactor and 3D simulations of a novel injection reactor with 19 inlet/outlet cells were performed. @FootnoteText@ @footnote 1@"Trends in aluminum etch rate uniformity in a commercial inductively coupled plasma etch system", JVST B 16(3), May/Jun 1998.

MS-ThP6 Reaction Products in a-C:H Film Growth by DC Glow Discharges in the Novillo Tokamak, ***R. Valencia***, Instituto Nacional de Investigaciones Nucleares (ININ), México*; J. de la Rosa,* Instituto Politécnico Nacional, México*; E. Camps, R. López,* ININ, México

In this work we report the reaction products generated during the growth of a-C:H films by DC glow discharges in a toroidal chamber using a calibrated mixture of 5 % methane and 95 % hydrogen and at a total pressure of 5x10@super-2@ Torr. The products were analyzed using a differentially pumped mass spectrometer. The time evolution of the partial pressure recorded after initiation of the glow discharges indicates that the reaction products are generated by the plasma-wall interaction. During the initial phase of the experiment, a continuous increase of the peak m/e=28 and a decrease of those at m/e=18, 32, and 44 was seen to occur. We suppose that the 28peak is principally due to CO because in the case of a carbonized surface, part of the initially deposited C atoms can form CO with surface oxides and the residual water vapor. The decrease of the peaks 18, 32 and 44 are due to a molecular dissociation of H@sub 2@O, O@sub 2, CO@sub 2. The films were characterized by X-ray diffraction and scanning electron microscopy. The thickness and refractive index of the films were determined from the interference fringes of the transmission spectrum.

MS-ThP7 Physically-based Dynamic Simulation of a Tungsten CVD Cluster Tool, *J.N. Kidder, Jr.,* ***N. Gupta****, G.W. Rubloff,* University of Maryland

Dynamic, physically-based simulation has proven effective in representing the time-dependent behavior of equipment, process, sensor and control systems. Here we extend previous work to address multichamber cluster tools and to include more complex pumping systems and models. Using a Windows-based simulation program, VisSim(tm) (Visual Solutions, Inc.), we have constructed and validated a system-level dynamic simulator for the Ulvac ERA-1000 tungsten CVD cluster tool at the Laboratory for Advanced Materials Processing, U. Maryland, in order to support research on chemical sensing, control, optimization, and fault management. The simulator reflects the time-dependent behavior of: the vacuum and gas handling components of the load lock, the buffer chamber, the process reactors, multi-stage gas pumping systems (e.g., mechanical and turbo pumps), and the gas delivery and exhaust systems; the process behavior in the reactor chambers; and the dynamics associated with process recipes. This enables the evaluation of dynamic process parameters (e.g., deposition rate, film thickness) as well as manufacturing parameters (e.g., cycle time), so that manufacturing figures of merit can be evaluated as a function of process and equipment design. Synchronous measurements of process variables and equipment state parameters provide experimental validation of the dynamic simulator.

MS-ThP8 Computer Simulation of Three-Dimensional Asymmetries in Inductively Coupled Plasma Reactors, ***T. Panagopoulos****, V. Midha, D.J. Economou,* University of Houston

MPRES-3D, a three-dimensional version of the Modular Plasma Reactor Simulator, has been developed to study azimuthal asymmetries of the etch rate introduced by gas injection and pumping ports, and by non-uniform power deposition profiles. The finite element method using higher order elements allows accurate representation of complicated reactor geometries. A 3-D Maxwell solver was also implemented to self-consistently account for azimuthal variations of the power deposition in the plasma. The chlorine plasma etching polysilicon was taken as a system for study. Gas inlets were found to introduce some local azimuthal asymmetries. In general, however, they did not contribute substantially to non-uniformities at the wafer level. The effect of pumping port(s) and non-uniform power absorption were more important since significant disturbances of all essential plasma species can be introduced. The implementation of a focus ring was found to yield practically azimuthally symmetric etching profiles. Overall, 3-D simulation tools are viewed as critically important for the design and optimization of upcoming 300 mm wafer plasma processing tools.

MS-ThP9 Ion Beam Deposition Systems for Highly Uniform Defect-free Coatings for Electronic Manufacturing Applications, ***A.V. Hayes****, H. Hegde, V. Kanarov, C.C. Fang, J. Wang, D. Kania,* Veeco Instruments, Inc.

Ion beam deposition (IBD) techniques are of increasing interest for use in the manufacturing of electronic devices. The most developed application is the production of high quality Extreme Ultraviolet (EUV) reticle masks.@footnote 1@ The IBD multilayer coatings generated by this work were very uniform, precisely deposited, and were lower in defects by several orders of magnitude compared to the best sputter deposited coatings. This has directly stimulated interest in extending the technique to the coating of advanced generation optical photomasks. On another front, recent advances have been made in the production of high quality Giant Magnetoresistive sensors using IBD methods. Such sensors are used in MRAM (Magnetic RAM) devices. In this work the ion beam deposition of low defect, uniform multilayer coatings with precisely controlled thickness, and of high quality magnetic films, is reviewed. This will be followed by a discussion of modeling and preliminary experimental data regarding extension of the technique for uniform coating of 300 mm substrates. @FootnoteText@ @footnote 1@S.P. Vernon, et al, Optical Society of America Trends in Optical Photronics, 4 (1996).

MS-ThP10 Estimation of the Ion Energy Distribution Function at Sputter Coils in PVD-IMP Systems, ***R. Veerasingam****, P. Gopalraja, E Kim, J.C. Forster,* Applied Materials, Inc.

Computer simulations were used to evaluate the ion energy distribution function (iedf) at the sputter coil of PVD-IMP systems. In the simulations, Ti/Ar and Ti/N2/Ar plasmas at 20 mTorr fill pressure were used to model the systems. The simulations revealed that in TiN systems, the plasma temperature and densities are lower compared to Ti systems. The existence of the excited states of nitrogen such as N* and N2*, provide an additional channel for electron energy dissipation rather than ionization and also lead to nitridization of surfaces. A TiN surface such as a nitridized sputter coil may have lower sputter yield compared to a pure Ti coil. By modifying the ion energy distribution function it is possible to enhance sputter yields from the coils. Control of the iedf at the coil surface provides a means to improve coil sputter and hence deposition uniformity. Experimental densities will be used to calculate the iedf. Results of the calculated plasma properties and iedfs will be presented.

Author Index

Bold page numbers indicate presenter