Wednesday Morning, November 4, 1998

Thin Films Division
Room 310 - Session TF-WeM

ULSI Metalization and Interconnects

Moderator: J. Hopwood, Northeastern University

8:20am **TF-WeM1 ULSI Metallization and Interconnects**, ***C.B. Whitman,*** CVC, Inc. **INVITED**

The performance of advanced IC chips is limited by the interconnect propagation delays, dispersion, and cross-talk within the Al/SiO@sub 2@ system. The combination of Cu and low-k dielectrics enables a reduction of the interconnect levels and improved reliability. Various deposition methods (MOCVD, PVD, and plating) have been evaluated for Cu. Vacuum-integrated clustering of single-wafer process modules offers advantages for advanced metallization applications. The capability to integrate the pre-clean process with the copper (seed and/or fill) and barrier layers in a vacuum cluster tool prevents atmospheric exposure of the sensitive metallization interfaces, resulting in improved process repeatability and reduced via resistance. A vacuum-integrated MOCVD metallization technology has been developed and demonstrated for formation of high-performance Cu plugs/lines for 0.18 - 0.13 µm IC manufacturing. MOCVD copper seed and gap-fill processes have been integrated with soft plasma clean and barrier deposition processes in a vacuum cluster tool. The MOCVD-Cu process is capable of void-free filling of high-aspect-ratio (up to 8:1) features with low-resistivity (@<=@2 micro-ohm.cm) Cu layers. Excellent copper layer adhesion and copper/barrier microstructure properties have been achieved. The films have shown negligible impurities and large (0.5 - 0.8 µm) grains with texturing. Deposition rates in the range of 400 to 3000 Å/min have been achieved. Inlaid MOCVD copper lines and vias have been fabricated with TiN and TaN barrier layers using CMP damascene processing. MOCVD-Cu offers performance advantages for fabrication of void-free inlaid lines/plugs for all the interconnect levels, including the lower levels with narrower and larger aspect-ratio lines and the upper interconnect levels with wider/thicker and smaller aspect-ratio lines. We have also demonstrated successful process integration of copper electroplating via/trench filling with MOCVD cluster tool barrier and seed formation.

9:00am **TF-WeM3 Pinhole Formation in Solid Phase Epitaxial Film of CoSi@sub 2@ on Si(111)**, ***L. Ruan,*** *D.M. Chen,* The Rowland Institute for Science

We have revisited the long-standing pinhole problem in solid phase epitaxial growth of a CoSi@sub 2@ film on Si(111) with in situ scanning tunneling microscopy.@footnote 1@ While the as-deposited film with 5 Å of Co at room temperature shows a smooth granular texture with original substrate terraces remaining intact, annealing at 580ºC produces an epitaxial CoSi@sub 2@ film with large pinholes enclosed by a thin ring CoSi@sub 2@, exhibiting a volcano feature. Quantitative analysis shows that the formation of pinholes is a result of rapid Si outward diffusion from bulk to surface, and of the subsequent Si reaction with Co on the outer surface. Evidence suggests that inhibiting the Si diffusion channels during the thermal annealing process is the key to solving the pinhole problem. @FootnoteText@ @footnote 1@Like Ruan and D. M.Chen, Apply. Phys. Lett. in press.

9:20am **TF-WeM4 Investigation of the Structural and Chemical Stability of Advanced Metal Gate and Ultra-Thin Gate Dielectric Interfaces**, ***B. Claflin,*** *G. Lucovsky,* North Carolina State University

Aggressive scaling of MOS device features to 0.1 µm and below will require the introduction of novel materials and new, low-thermal-budget processes. For example, in front end-of-the-line processing, alternative gate dielectrics such as ultra-thin SiO@sub 2@/Si@sub 3@N@sub 4@ stacks and/or high dielectric constant (K) materials such as Ta@sub 2@O@sub 5@ will be required to scale down the oxide equivalent thickness, t@sub ox@, and limit leakage current to acceptable levels. Likewise, replacements for heavily doped polycrystalline Si (poly-Si) gate electrodes such as simple or compound metals will be needed to prevent i) poly-depletion and ii) boron out-diffusion and dielectric penetration effects. However, the compatibility of these new materials under device processing conditions must be demonstrated. For example, many transition metals chemically react@footnote 1,2@ with SiO@sub 2@ at temperatures above 650@degree@C, and as such can not be used in gate stacks. In addition, the effects of thin film microstructure or phase transitions can dramatically alter the electronic and mechanical properties of these materials, and their interfaces, degrading both device performance and reliability. Recent studies@footnote 3,4@ indicate that TiN@sub x@ and WN@sub x@ composite metal gates are compatible with ultra-thin remote plasma-enhanced chemical-vapor deposited (RPECVD) SiO@sub 2@ and stacked SiO@sub 2@/Si@sub 3@N@sub 4@ gate dielectrics that are subjected to rapid thermal annealing (RTA); i.e., they perform well as metal gate electrode in MOS device structures. In this work, the structural integrity of these metal/dielectric interfaces subjected to RTA is investigated by SEM, TEM, and X-ray diffraction. These structural characterizations are correlated with the chemical stability of these interfaces determined by Auger electron spectroscopy (AES). Supported by NSF, SRC, and ONR. @FootnoteText@ @footnote 1@ S. Q. Wang and J. W. Mayer, J. Appl. Phys. 64, 4711 (1988). @footnote 2@ R. Pretorius, J. M. Harris, M-A. Nicolet, Solid State Electron. 21, 667 (1978). @footnote 3@ B. Claflin, M. Binger, and G. Lucovsky, J. Vac. Sci. Technol. A 16 (1998), in press. @footnote 4@ B. Claflin, M. Binger, and G. Lucovsky, Mat. Res. Soc. Symp. Proc. (1998), in press.

9:40am **TF-WeM5 Low Temperature Deposition of Zirconium Diboride, A Candidate Diffusion Barrier, Using Remote Plasma CVD**, ***J.H. Sung,*** *D.M. Goedde, G.S. Girolami, J.R. Abelson,* University of Illinois, Urbana-Champaign

Zirconium diboride is potentially suitable as an advanced diffusion barrier in ULSI circuits because of its low electrical resistivity, 10 micro-ohm-cm in bulk form, very high melting temperature, ~ 3000 C, and resistance to air oxidation and reaction with metals. However, the CVD of ZrB2 from conventional halide/hydrogen source gases requires a relatively high temperature of ~ 900 °C. We showed that zirconium tetrahydroborate, Zr(BH@sub 4@)@sub 4@, is an attractive precursor which has high vapor pressure and can be thermolyzed at < 300 °C to produce ZrB2 films with resistivity ~ 120 µm@OMEGA@-cm. In this work, we report the use of remote plasma CVD to further reduce the ZrB2 deposition temperature and improve the film properties. Atomic hydrogen is generated by a microwave plasma source and mixed downstream with Zr(BH@sub 4@)@sub 4@ to produce high quality films at only 150 °C. The films have resistivity ~ 60 µm@OMEGA@-cm, and low carbon and oxygen contamination. XPS data indicate that the plasma-deposited films are single phase ZrB2. Based on in-situ mass spectroscopy data, we will present a preliminary analysis of the chemical reaction pathways associated with the remote plasma growth process.

10:00am **TF-WeM6 A Parameter Free Model for the Simulation of Trench Filling Profiles under Al PVD and Al IPVD Conditions**, ***A. Kersch,*** Siemens Ag, Germany*; U.P. Hansen,* Technical University Munich, Germany

Simulation results are presented for microscopic profile evolution of deposited Al metal films in trench structures. The model for the simulation is derived from atomistic, molecular dynamics calculations using a previously developed Al-Al interaction model.@footnote 1@ The essential elements are: (1) an angular and energy dependent non unity sticking coefficient resulting in specular reflection of the impinging Al atoms, (2) an energy and angular dependent sputter yield. The parameters of the model are obtained from the molecular dynamics results, surface diffusion is so far neglected. We study the surface evolution and sidewall coverage for different PVD and IPVD conditions for trench structures of different aspect ratios and clarify the influence of the model elements on the deposition process. The predictions of the model agree with the results of a published model@footnote 2@ in some range of process conditions. Finally results are compared to experimental data. @FootnoteText@ @footnote 1@U. Hansen, Molecular Dynamics Study of Al PVD Processes @footnote 2@S. Hamaguchi and S.M. Rossnagel, J. Vac. Sci. Technol. B13 (1995) 183

10:20am **TF-WeM7 Energy Dependent Atomistic Simulations of Trench-filling**, ***Y.G. Yang,*** *X.W. Zhou, H.N.G. Wadley,* University of Virginia

A comprehensive atomistic analysis of incident kinetic energy effects during vapor deposition has been conducted and the results integrated into a kinetic Monte Carlo simulation of physical vapor deposition. Interactions of hyperthermal atoms with substrate that resulted in biased diffusion, atomic reflection, resputtering and local thermal spikes were incorporated in a simulation model that also included normal, thermally driven multipath diffusional processes. Results are presented for the vapor phase deposition of metal interconnects by the dual damascene process. This involves the filling of increasingly narrow trenches with copper and other metals. Filling of these trenches has been studied as a function of the substrate temperature, the deposition rate, trench geometric parameters, incident atom flux energy and angular distributions.

10:40am **TF-WeM8 Sputtered Copper Seedlayer Processing Issues**, ***E.C. Cooney III,*** *D.C. Strippe, J.W. Korejwa, A.H. Simon, C. Uzoh,* IBM Microelectronics

One method to produce reliable Copper interconnects for advanced logic chip technology utilizes sputtered Copper seedlayers which are subsequently electroplated. However, experimental results indicate that good film step coverage as well as conformality are necessary to promote complete filling of the feature. Current trench dimensions and dual damascene aspect ratios are such that traditional sputter processes cannot adequately cover these structures. In addition, Copper tends to dewet from the substrate when thermal aspects of the process, such as sputter energy and deposition temperature, become too great. This can lead to a discontinuous film causing void formation during electrodeposition. We have investigated collimation of Copper films to improve the conformality in aggressive single and dual damascene structures. Collimation filters of various aspect ratio were used to deposit Copper seedlayers which were then filled using electrodeposition. In addition, thermal effects were examined through experimentation with lower DC magnetron powers coupled with special platen cooling considerations to reduce the heat load within the film. Electrical opens-yield and resistance data was then measured. Failure analysis was also performed to observe the plating fill.

11:00am **TF-WeM9 The Effect of Sputter Process and Target Pass-Through Flux on Sputter Deposition of Co Thin Film for Cobalt Silicide Metallization**, ***H. Zhang***, *J. Poole, R. Eller, M. Keefe,* Tosoh SMD, Inc.

CoSi@sub 2@ is considered an alternative to TiSi@sub 2@ for use as a contact in ULSI due to its low resistivity, excellent chemical stability and lower formation temperature. Sputter deposition of Co thin film is one of the crucial steps in salicide (self-aligned silicide) process. One major problem with sputter deposition of Co thin film, however, is that Co is a ferromagnetic material, which can be difficult to sputter. Magnetic field strength has been found to be the key parameter in sputtering magnetic films. In magnetron sputtering of Co, high magnetic field strength can be obtained by using a high pass-through flux (PTF) target that allows maximum magnetic flux from the magnets to permeate through the magnets. A high PTF target also allows efficient sputtering and uniform target erosion. The effects of target PTF and sputtering process parameters such as Ar pressure, sputtering power, target to substrate spacing and substrate temperature on the sputter process and film properties were studied. Co targets with PTF of 65% (high PTF), 55% (medium PFT) and 35% (low PTF) were sputtered. Co thin films ranging from 16 nm to 500 nm in thickness were deposited on 200 mm (100) Si wafers. Sputter deposition rate, I-V characteristics, film sheet resistance and film uniformity was measured under various sputter conditions. It is indicated that the I-V characteristics of different PFT targets followed the normal I=KV* relationship of DC planar magnetron sputtering. The exponents in the equation, n, increased with increasing target PTF, indicating the higher the PTF, the lower the impedance. The target having the highest PFT demonstrated the best film uniformity. Rapid thermal processing was carried out to form cobalt silicides at temperatures between 300°C to 850°C in Ar ambient for various times. The sheet resistance of the Co and cobalt silicide films was monitored by four-point probe before and after the RTP. Phases and microstructure of the films were characterized using XRD, SEM and SIMS. The sheet resistance decreased significantly after annealing at 600°C and 700°C due to formation of CoSi@sub 2@, which has lower resistivity. The significant increase in sheet resistance after annealing at 400°C and 500°C was attributed to formation of CoSi phase. For the 16 nm thick Co film, sheet resistance of 3.2 @OMEGA@/sq was obtained after RTP at 600°C and 700°C.

11:20am **TF-WeM10 Improvement of Morphological Stability of Ag Thin on TiN Layer**, ***C.-Y. Hong***, Massachusetts Institute of Technology*; Y.-C. Peng, L.-J. Chen,* National Tsing-Hua University, Republic of China*; W.-Y. Hsieh,* United Microelectronic Corporation, Republic of China

Owing to the need to increase the packing density in ULSI, thermally stable low-resistive contact and metallization technologies are important. Numerous studies of noble-metal-semiconductor processes have been conducted to obtain a better understanding of the interface structure and other properties. Ag is the most conductive materials and has been considered to be a candidate materials for interconnection in ULCI fabrication. Since fast interdiffusion occursbetween Ag and Si substrate, advanced metallization technologies of Ag for ULSI require a highly comformal barrier layer to prevent the interdiffusion between Ag and Si substrate. Among various kinds of diffusion barriers, titanium nitride (TiN) thin films have been widely used in ULSI fabrication due to its relatively low electrical resistivity and high thermal stability. In a previous study, Ag islands were found to form on TiN layers after annealing at 100 °C for 30 min. Owing to the poor morphological stability of the Ag/TiN interface, the utilization of thin Au and Ti layers between Ag and TiN layers has been explored to overcome the island formation problem in this study. The presence of interposing Au and Ti layers was found to increase the morphological stability temperature of Ag thin films on TiN layer from 100 °C to 450 °C and 350 °C, respectively.

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