Wednesday Morning, November 4, 1998

Plasma Science and Technology Division
Room 318/319/320 - Session PS-WeM

Plasma Damage

Moderator: J. Werking, Sematech

8:20am **PS-WeM1 Gate Oxide Damage: Testing Approaches and Methodologies**, ***C.T. Gabriel,*** VLSI Technology, Inc. **INVITED**

Plasma processing of MOS devices has the potential to induce damaging current flow through thin gate oxides. Many studies have undertaken to measure this damage, using what at first appears to be a bewildering variety of measurement techniques. A natural question to ask is, which measurement technique is best? Can't the industry standardize on a particular technique? Actually, to study gate oxide damage, a variety of complementary techniques is needed. There are two broad families of gate oxide damage measurement techniques: those that characterize the charging source independent of the gate oxide, and those that characterize the effect of the damage by examining gate oxide degradation. To study the damaging potential of the plasma itself, measurement devices include EEPROM transistors, MNOS transistors, contact potential difference, and direct measurement techniques. To study the effect that plasma damage has on gate oxide, electrical parameters are measured appropriate for capacitors and transistors, which are typically connected to large, conductive "antennas" over thick field oxide. To select the proper measurement technique, one must first have a fundamental understanding of the damage mechanism. Charging during plasma processing arises from two main sources: plasma nonuniformity and electron shading. Plasma nonuniformity is relatively independent of the wafer, so a wide variety of techniques can be used to predict or detect damage resulting from it. However, electron shading is essentially an interaction with structures on the wafer, so damage detection is critically dependent on the measurement technique. The options for measuring gate oxide damage will be reviewed and compared, leading to a selection of "application-specific" damage measurement techniques.

9:00am **PS-WeM3 Evaluation of Charging Damage Test Structures for Ion Implantation Processes**, ***M.J. Goeckner,*** *S.B. Felch, J. Weeman, S. Mehta,* Varian Associates*; J.S. Reedholm,* Reedholm

Charging damage is a critical issue in both current and future ion implantation systems. In conventional ion implanters, plasma flood guns have been used successfully to reduce charging damage. However, the development of sub-0.18 µm devices will make control of wafer charging more important. In addition, sub-0.18 µm devices will require novel doping technologies such as ultra-low energy (ULE) ion implanters or plasma doping (PLAD). Throughput requirements for these new technologies, and other issues, might also make charging damage more prevalent. Because of these concerns, we are examining the efficacy of two charging test structures. They are Varian Research Center's (VRC) proprietary charging test structures@footnote 1@ and the test structures on CHARM-2 wafers.@footnote 2,3@ These test structures operate on two very different principles. The VRC test structures use static "antenna" MOS capacitors, while the CHARM-2 uses programmable EEPROM's. Each system has distinct limitations and advantages. For example, the CHARM-2 wafer can be used to measure the maximum induced surface voltage; however the result is influenced by the elapsed time between programming, exposure and data collection. In comparison, the VRC result is static, but the precise value of the induced surface voltage can not be measured. Both structures will be put through a series of tests on both PLAD and traditional implanters. Comparisons will be made of sensitivity, temporal and spatial variability, as well as any potential limitations or advantages each might have for examining charging in ULE and PLAD implantation environments. @FootnoteText@ @footnote 1@S.B. Felch and S. Mehta in "Materials and Process Characterization of Ion Implantation," Edited by M.I. Current and C. B. Yarling, (Ion Beam Press, Austin TX, 1997), pp 288-295. @footnote 2@W. Lukaszek in "Materials and Process Characterization of Ion Implantation," Edited by M.I. Current and C. B. Yarling, (Ion Beam Press, Austin TX, 1997), pp 296-317. @footnote 3@CHARM-2 is a registered trademark of WCM.

9:20am **PS-WeM4 SPORT Measured Electron Shading Effects and Comparison with Computer Simulation**, ***S.C. Siu,*** *R. Patrick, V. Vahedi,* Lam Research Corporation

Electron shading is recognized as a major mechanism for plasma processed induced damage in commercial plasma etch chambers. As the semiconductor industry moves to smaller feature sizes and thinner gate oxides, shading induced damage becomes a greater concern. The shading effect is known to be more severe with higher aspect ratio features and high density plasmas. This study uses SPORT wafers to measure plasma parameters and the shading effect in a commercial plasma etcher. The advantage of using a SPORT wafer is that the plasma measurements are at the wafer surface. The SPORT wafer was used as a planar floating asymmetric double probe. Ion and electron currents were collected and the electron energy distribution calculated. Measurements were also done with patterned pads of different aspect ratio features. Differences in the ion and electron current were clearly seen between a bare and shaded pad. A PIC simulation was used to predict shading effects. The simulation is able to account for charged resist structures that cause electron shading. Comparisons were made between the simulation and the experimental results.

9:40am **PS-WeM5 Suppression of Charging Damage Caused by Electron Shading Effect in Gate Etching Technology**, ***K. Yoshida,*** *K. Tokashiki, H. Miyamoto,* NEC Corporation, Japan

Recently, the charging damage caused by electron shading effect has become a serious problem in etching processes using high-density low-pressure plasma. This effect causes profile distortion and/or gate oxide degradation. It is expected that these problems would be enhanced in sub-quarter-micron device fabrication because of their high aspect ratios. We reported in American Vacuum Society 44th National Symposium(PS-MoM8) that the profile distortion was suppressed by applying the high pressure(@>=@20 mTorr) and low source power in HBr gas plasma to over-etching step for 0.18 µmm gate etch process. Furthermore we have studied the correlation between the profile distortion and the gate oxide degradation in order to suppress the charging damage successfully. The impact of gas chemistry (Cl@sub 2@ and HBr) and pressure on charging damage was evaluated in gate etching. Especially we focused on the just and over etch period because the charging damage takes place in this period. Thickness of gate film and that of gate oxide were 200 nm and 4.5 nm, respectively. An initial-electron-trapping-rate (IETR) method was applied to monitor the charging damage. We measured dV/dt slope under 40 mA/cm@super -2@ stress current with antenna ratios ranged from 50 to 66,700. At low pressure (2 mTorr) Cl@sub 2@ and HBr plasmas, dV/dt slope increased significantly as the antenna ratio were over 10,000. The dV/dt reached about 10 mV/sec, which means serious damage took place. However, as increasing in pressure, dV/dt slope or charging damage was effectively suppressed (dV/dt@<=@2 mV/sec at 20 mTorr). It was also found that HBr plasma more effectively suppressed the damage than Cl@sub 2@ plasma. Interestingly, these damage test results corresponded to the dependence of the profile distortion on gas chemistry and pressure. One of reasons for the different damage result between Cl@sub 2@ and HBr correlates with the different plasma characteristics between them. Electron temperature(T@sub e@) and density(N@sub e@) for Cl@sub 2@ plasma were higher than that of HBr plasma at the pressure ranged from 2 to 20 mTorr. T@sub e@ and N@sub e@ decreased with increasing pressure, 4.2 to 2.9 eV of T@sub e@ and 2.5E10 to 9.5E9 cm@super -3@ of Ne for Cl@sub 2@ plasma. In HBr plasma, T@sub e@ and N@sub e@ were lowered to 2.6 eV and 4E9 cm@super -3@ at 20 mTorr. In conclusion, the gate oxide degradation caused by electron shading effect correlates with the profile distortion. And the use of relatively high pressure(@>=@20 mTorr) HBr plasma in just and over etch period is useful to suppress the charging damage caused by electron shading effect.

10:00am **PS-WeM6 Modeling of Charging Damage during Dielectric Deposition in High-Density Plasmas**, *G.S. Hwang,* ***K.P. Giapis,*** California Institute of Technology

The mechanism of charging up of interconnect metal lines during interlevel dielectric (ILD) deposition in high-density plasmas is investigated by detailed and self-consistent Monte Carlo simulations of pattern-dependent charging.@footnote 1@ The results suggest that the initial conformality of the ILD film plays a crucial role in metal line charging up and the subsequent degradation to the buried gate oxide to which the metal line is connected. Line charging occurs when the top dielectric is thick enough to prevent tunneling currents while the sidewall dielectric thickness still allows tunneling currents to flow to the metal line; the differential charging of the sidewalls, which induces the latter currents, is caused by electron shading. The simulations include a treatment of charge dissipation along the surface of the dielectric;@footnote 2@ surface currents can significantly decrease the cumulative charging damage when facile at small surface potential gradients. Charging damage during plasma-assisted ILD deposition could become a problem more serious than that occurring

during plasma etching and is expected to pose additional requirements to low-k dielectrics currently sought to replace SiO@sub 2@. However, under the assumptions considered, a dramatic reduction in charging damage can be accomplished by depositing a more conformal ILD film around the metal line and/or by increasing the ability of the film surface to dissipate charge. @FootnoteText@ @footnote 1@ G. S. Hwang and K. P. Giapis, J. Appl. Phys., Vol. 84, to appear on July 1, 1998. @footnote 2@ G. S. Hwang and K. P. Giapis, Appl. Phys. Lett., Vol. 71, 458 (1997).

10:20am **PS-WeM7 Silicon Oxidation Employing Negative Ion under Transformer Coupled RF Bias**, ***H. Shindo***, *T. Fujii, T. Koromogawa,* Tokai University, Japan*; Y. Horiike,* Toyo University, Japan

Directional silicon oxidation technique is highly required in various ULSI processes. Especially for trench isolation of memory cell, the oxidation should be directional but with low damage. For this purpose, a new method of negative ion assisted silicon oxidation has been experimentally studied employing a microwave O@sub 2@ plasma. A feasibility of directional silicon oxidation by negative ion was examined. The plasma produced in a 6 inch stainless-steel chamber was employed and the downstream plasma was mainly concerned because the negative ion was highly populated. Ion mass and energy analysis showed that the dominant negative ion was O @super -@ and its density was more than one order higher than O @sub 2@@super -@. The oxide film quality produced was analyzed by XPS, FTIR and ellipsometer. The oxidation depth under the positive DC biases without any local discharge showed a great voltage dependence, meaning a major role of negative ion O @super -@ for oxidation. While under the negative DC biases the oxidation was rather small but the fairly large amount of the sputtering was observed at the voltage as small as 50 V, indicating the high chemical reactivity of O @super -@. In conjunction with the sputtering, however, it was observed that the sputtering became remarkable in a condition of oxidation saturation. On a basis of the oxidation depth obtained under these DC biases, directional oxidation was examined under low frequency RF bias of 100 kHz with a transformer couple to apply the net positive voltage for negative ion. This directional oxidation was made employing a Si sample of line and space with SiO@sub 2@ mask. It was demonstrated that the directional oxidation of1500A depth was possible under the RF bias of 25 W with 10 minute.

10:40am **PS-WeM8 Direct Measurement of VUV Caused Oxide Conduction during Plasma Charging**, ***J.P. McVittie***, Stanford University

In a plasma the local charging voltage of a floating structure is controlled by the difference in local electron and ion fluxes, the local capacitance and the feedback of the developed voltage on the local plasma sheath, which controls the electron current. Any additional discharging current paths will also affect the charging voltage and subsequent device damage. One such current path which is poorly understood is UV induced photoconductivity in dielectrics. Among of the problems in understanding this discharging path has been the difficulty in measuring dielectric conduction in a plasma and in separating charging from UV effects. In his work a very low density plasma was used to induced charging up to 20 V while a separate high density plasma separated by a thin filter/window was used to generate the vacuum UV. For monitoring charging a bare SPORT charging probes were used, and to monitor photoconductivity oxide covered probes were used. Conductivity which deceased linearly with the UV source power was observed. In addition, the conductivity deceased with 1/ oxide thickness squared. Finally, by using different filters it was concluded that VUV near the oxide band gap of ~9 eV was causing the conductivity. All these observations are consistent classic bulk induced photoconductivity. The implications of this dielectric conductivity on charging and related damage will be discussed.

11:00am **PS-WeM9 Vacuum Ultraviolet Spectra of Metal-Etch Plasma Processing Discharges**, ***J.R. Woodworth***, *M.G. Blain, R.L. Jarecki,* Sandia National Laboratories*; T.W. Hamilton,* Sandia National Laboratories, U. S. A*; B.P. Aragon,* Sandia National Laboratories, U. S. A.

We report measurements of the absolute fluxes of vacuum ultraviolet (VUV) photons to the wafer in a commercial aluminum-etch inductively coupled plasma processing tool for discharges containing chlorine, boron trichloride and argon. Most of the VUV emissions that we observed above 8 eV in these discharges were due to spectral lines of neutral chlorine atoms. Spectra and absolute fluxes as a function of rf power, substrate type, gas mixture, and pressure will be presented. This work was supported by the United States Department of Energy Under Contract No. AC04-94AL8500, by SEMATECH, and by Applied Materials. Sandia is a multiprogram laboratory operated by the Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy.

11:20am **PS-WeM10 Spatial Characterization of Plasma VUV Emission in an ECR Etcher**, ***C. Cismaru***, *J.L. Shohet,* University of Wisconsin, Madison

In MOS (Metal-Oxide-Semiconductor) device fabrication, plasma processing plays an important role since it has many advantages in terms of process convenience, directionality and high resolution. However, because of the existence of charged particles, together with x-ray and vacuum ultraviolet emission, plasma processing enhances the possibility of damage of the processed materials. The damage potential of vacuum ultraviolet emission of processing plasmas on MOS devices is investigated. High energy photons, with energies higher than the energy band gap of SiO@sub 2@ (~9 eV) can be generated from recombination and relaxation processes in the plasma. It has been established that electron-hole pairs generated in the oxide by these photons@footnote 1@ will increase the SiO@sub 2@ bulk and Si/SiO@sub 2@ interface trapped-charge density, which will affect the device quality accordingly.@footnote 2@ In this work, emission spectra of various plasmas have been recorded in an ECR (Electron Cyclotron Resonance) etcher, at pressures ranging between 0.5 mTorr and 5 mTorr, and microwave powers between 700 W and 1000 W. The measurements were taken in the range of 20 Å to 3000 Å (600 eV to 4 eV), with a one-meter normal incidence vacuum monochromator, with a resolution of 0.2 Å. By use of a special reflection probe, the spectra were also recorded as a function of position across the wafer stage. The measurements show that most of the VUV emission of processing plasmas ranges above 9 eV, which may result in a potentially damaging effect on MOS devices. Also, a nonuniformity of the VUV photon flux impinging on the wafer surface as a function of position across the wafer has been found. This nonuniformity should be considered as having the potential for another MOS processing damaging factor. This work was supported in part by the National Science Foundation under Grant No. EEC 8721545. @FootnoteText@ @footnote 1@ R. A. Gdula, IEEE Transaction on Electron Devices 26(4), 644 (1979). @footnote 2@ R.J. Powell and G.F. Derbenwick, IEEE Transactions on Nuclear Science 18(6), 99 (1971).

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