Plasma Science and Technology Division
Room 318/319/320 - Session PS+MS-TuA

ULSI Technology

Moderator: M. Liehr, IBM T.J. Watson Research Center

2:40pm **PS+MS-TuA3 Front End Integration for ULSI Technologies**, ***W.A. Mueller,*** SIEMENS Microelectronics, DRAM Development Alliance, Germany **INVITED**

Key frontend integration challenges for sub 0.25 µm technologies will be discussed. For device isolation shallow trench isolation (STI) has emerged as the main road; the different approaches for STI fill and planarization will be evaluated. For the transistor integration shallow retrograde wells, sub 5 nm gate dielectrics, dual work function gates and shallow source/drain junctions are the key technologies. Logic and DRAM applications are posing different boundary conditions for integration, thus leading to different solutions for the device architecture. For high packing density memory arrays and cell based designs selfaligned contact- and local interconnect schemes has to be integrated in the frontend process flow. As a DRAM specific topic the integration challenges for trench- and stack capacitors will be addressed.

3:20pm **PS+MS-TuA5 Transient Diffusion Effects in Silicon Technology**, ***C.S. Rafferty,*** Bell Laboratories, Lucent Technologies **INVITED**

In modern silicon technology, there is a steady trend to reduce the "thermal budget" of fabrication processes. The intent has been to reduce the thermal diffusion of dopants. However low temperatures have exposed significant non-equilibrium diffusion effects. The most striking of these, transient enhanced diffusion, causes many unexpected influences on devices. Transient diffusion (TED) is the enhanced diffusion rate of dopants due to point defects introduced during ion implantation. The enhancement can be as much as four decades above thermal diffusion rates. TED by its nature is cooperative in nature, where implanting one species can lead to enhanced diffusion of all the other species in the wafer, even those located some distance from the implantation window. The effects of such local and remote diffusion transients on transistors is manifold. In some cases, the transistors may fail completely to function as intended, in others, their properties may be degraded or shifted from their intended targets. This talk describes some of the experimentally observed impacts of transient diffusion in technology. It is shown how a better understanding of the materials science involved can lead to better devices.

4:00pm **PS+MS-TuA7 Technology Requirements for Logic ICs**, ***M. Brillouët***, France Telecom, France **INVITED**

The logic ICs are targeting an higher packing density for increased performances and cost effective manufacturing. In the ‘front-end’ part of the process (i.e. the transistor and the lateral isolation), this higher integration is obtained - along with higher operating frequencies and reduced power consumption - in shrinking the feature sizes. As the materials stay basically the same (i.e. Si and SiO@sub 2@), this trend stresses strongly the photolithographic techniques : the etch process has to define structures at the atomic level ; selectivity, CD and profile are key parameters to control in these features with such an high aspect ratio. The density of the interconnections (‘back-end’ part of the process) can be improved by shrinking the feature sizes and by increasing the number of metal layers. Unfortunately, if one stays with the classical Al/SiO@sub 2@ system, while shrinking the metal pitch, the performance of the integrated circuit is degraded : there is thus a growing need to move to new materials (e.g. dual Damascene copper lines and insulators with a lower dielectric constant). Advanced developments will be required in the etching of these materials and, due to the introduction of the Damascene approach, the equipment set will be radically changed in a manufacturing line. The metallisation process impacts strongly the behaviour of the transistor : plasma induced damage during processing degrades the active devices and specific care need to be taken in order to minimize this detrimental effect. Finally, as the number of metal levels is increased, manufacturability is a major issue in the cost of the final product: improving the defectivity level of the interconnects is a key point, as more than half the process steps are now involved in the fabrication of the interconnection system.

4:40pm **PS+MS-TuA9 Advanced Deep-UV and 193 nm Optical Lithography: The Role of Resists, Reflectivity Control and Resolution Enhancement Technologies**, ***O. Nalamasu,*** *R.A. Cirelli, G.P. Watson,* Bell Laboratories, Lucent Technologies **INVITED**

The fabrication of integrated circuits with optical lithography faces several challenges as the industry is moving from I-line to deep-UV and 193 nm lithographies. For the immediate future, the technical challenges in developing manufacturing processes with k values below 0.5 have been identified and are the subject of intense R&D activity across the world. The low k lithography solution requires fundamental understanding of, as well as innovations in optical and resist materials, reflectivity control and resolution enhancement (mask and optical) techniques. In this presentation, we will detail our research efforts in Resist materials, Reflectivity control and Resolution enhancement techology areas with special emphasis on 193 nm lithography and identify the issues and opportunities in extending the optical lithography for patterning sub-0.1 µm devices. We will also demonstrate 60 nm resolution with 193 nm lithography by combining research advances in single layer resist, dielectric anti-reflective layer/hard mask with a levenson phase-shifting mask.

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