Wednesday Afternoon, November 4, 1998

Manufacturing Science and Technology Group
Room 317 - Session MS-WeA

Process Control and Yield from Tool to Factory

Moderator: S. Shankar, Intel Corporation

2:00pm **MS-WeA1 Factory Implementation of Process Control: Technical or Cultural Challenge?*, K.G. Vickers,*** Texas Instruments **INVITED**

The use of systematic, company wide process control techniques in integrated circuit manufacturing factories (known as wafer fabs) have been low since the inception of the industry in the 1960s. Reasons for this low implementation of process control methods have included both technical and cultural barriers to implementation. The technical barriers that have hampered process control implementation in wafer fabs originated from both the unique nature of IC fabrication processing and the rapidly changing equipment sets needed to build ever advanced technology node integrated circuits. These technical barriers included the simultaneous continuous flow and discrete event nature of most processes, the high number of equipment types/processes in an IC product flow, the significant changes in required process output from run to run, and the lack of computing power to handle a large diversified data stream. In recent years these technical barriers been reduced to the point that the size of the cultural barriers have become obvious as the major obstacle to successful systematic implementation. These cultural barriers originated in early wafer fabs whose technical population was strongly focused on device characteristics rather than process stability, whose reward and recognition system was based on local problem solutions rather than systematic solutions, and whose manufacturing methods were created locally rather than through company wide standardization. Over the last fifteen years Texas Instruments has achieved some success in overcoming first the technical barriers and then the cultural barriers for systematic implementation of advanced process control techniques in all TI world wide wafer fabs. This presentation will highlight the necessary technical changes that were put in place, and a key set of cultural changes that were implemented, to gain the benefits of systematic process control in a world wide manufacturing environment.

2:40pm **MS-WeA3 Advanced Process Control and Sensor Requirements for Reducing Non-Product Wafer Usage and to Increase Tool OEE in 300mm Manufacturing*, M.L. Passow,*** *J. Pace,* IBM Corporation **INVITED**

To maintain productivity in leading edge manufacturing, shrinking feature sizes and increases in equipment productivity are necessary. The shift from 200mm diameter wafers to 300mm diameter wafers is required, but not sufficient. Improvements in equipment OEE and reductions in the usage of non-product (NP) wafers and SAHD wafers must be made as the cost of using conventional methods of control in new, fully automated 300mm fabs is too high. Based on learning gained by understanding NP wafer usage in 200mm development and manufacturing lines, areas with the highest potential benefit from various reduction strategies will be identified. Process tool suppliers will be requested to incorporate Advanced Process Control (APC) strategies where possible. Adherence to standards will be required to facilitate the adaptation of new sensor, APC, data collection, and line management strategies to meet these needs. Particular recommendations will be presented.

3:20pm **MS-WeA5 Process Module Control Technology for 300mm Plasma Processing*, F. Kaveh,*** *B. McMillin, W. Collison,* Lam Research Corporation **INVITED**

In order to meet the challenge posed by the processing of the 300mm wafers, and the move toward sub quarter micron feature sizes, a new hybrid etch tool control architecture has been devised. This new architecture, based on TI's ControlWORKS environment, has enabled close coupling of a number of feedback loops for control of equipment level parameters, as well as control of stand alone remote sub-systems. Through the use of VME based direct I/O, for fast loops, and LonWorks network for less time critical loops, effective partitioning and optimization of the control functions has been achieved . Through the digitization and integration of a number of the process control loops such as the match and pressure controllers, measurable improvements in the overall operation of the tool has been realized. Further, a structure has been put in place that allows further integration of the aforementioned loops, and implementation of outer loops, for plasma state control applications. The new architecture is highly flexible, and as such, has enabled the integration of various sensors, such as an optical emission spectrometer, and a low cost RGA. These sensors are being used for detailed characterization of the chamber and the plasma, and are expected to result in significant gains in tool productivity and performance.

4:00pm **MS-WeA7 Using Wafermap Data for Automated Yield Analysis@footnote 1@*, K.W. Tobin,*** *T.P. Karnowski, S.S. Gleason,* Oak Ridge National Laboratory*; D. Jensen, F. Lakhani, C. Long,* SEMATECH **INVITED**

To be productive and profitable in a modern semiconductor fabrication environment, it is required that large amounts of manufacturing data be collected and maintained. This includes data collected from in-line and off-line wafer inspection systems and from the process equipment itself. This data is increasingly being relied upon to design new processes, control and maintain tools, and to provide the information needed for rapid yield learning and prediction. Because of increasing device complexity, the amount of data being generated is outstripping the yield engineer's ability to effectively monitor and correct unexpected trends and excursions. The 1997 SIA National Technology Roadmap for Semiconductors highlights a need to address these issues through "automated data reduction algorithms to source defects from multiple data sources and to reduce defect sourcing time." In this paper, we will discuss the current state of yield management automation and the role that SEMATECH and the Oak Ridge National Laboratory@footnote 2@ are taking in directing and developing new technologies that will provide the yield engineer with higher levels of automated data reduction and analysis. Yield management systems have been evolving over the past decade from a primary role of database storage and retrieval to systems that provide timely insight into the current state of manufacturing. The evolutionary process can be described in terms of five fundamental steps: (1) infrastructure and database management; (2) processes that add context to the data, i.e., that add information; (3) the use of data and context to find patterns, i.e., extract information; (4) methods of interpreting patterns, i.e., extracting knowledge; (5) and the automated application of process knowledge to yield management. In this paper we will focus on step (2), technologies which add context to data. In particular, we will discuss ORNL's contributions to the fields of automatic defect classification (ADC) and whole-wafer spatial signature analysis (SSA) for optical and electrical test data. We will also discuss preliminary results in the field of manufacturing-specific, content-based image retrieval (MSCBIR). MSCBIR is an image-based datamining technology that allows engineers to search a large image repository using an image of a semiconductor defect event as a query to locate other images that are similar in appearance. This exciting new technology is valuable due to the highly image-oriented approach taken by the yield engineer in problem solving, and the vast quantities of images stored in yield-management databases (approximately 70% of the total data). The ability to automatically extract content from raw manufacturing data will be a key factor for automating the discovery of knowledge in the dynamic semiconductor manufacturing environment. The current state of the art in yield management is only now beginning to comprehend these capabilities. Potential future applications of this knowledge in areas such as auto-sourcing statistical process control, condition-based maintenance of process tools, and yield prediction will also be briefly presented. @FootnoteText@ @footnote 1@K.W.T. (Correspondence): E-mail tobinkwjr@ornl.gov; WWW: http://www-ismv.ic.ornl.gov; Telephone: (423) 574-8521; Fax: (423) 574-6663. @footnote 2@Work Performed for SEMATECH, Austin Texas, under Contract No. ERD-95-1340 and prepared by OAK RIDGE NATIONAL LABORATORY, Oak Ridge, Tennessee, 37831-6285, managed by LOCKHEED MARTIN ENERGY RESARCH CORP. for the U.S. DEPARTMENT OF ENERGY under contract DE-AC05-96OR22464. @footnote 3@ K.W. Tobin, S.S. Gleason, F. Lakhani, and M.H. Bennett, "Automated Analysis for Rapid Defect Sourcing and Yield Learning", Future Fab International, Issue 4, Vol. 1, Technology Publishing Ltd., London 1997, p. 313.

4:40pm **MS-WeA9 Visual Data Mining of Defectivity Data using Parallel Coordinates*, A. Chatterjee,*** IBM Research **INVITED**

Defectivity data from a 4MB DRAM manufacturing process was analyzed using a visual data mining methodology based on Parallel Coordinates. Parallel Coordinates provides an interactive framework for analyzing multi-variate data graphically using 2-D graphs that can be colored using visual queries. These graphs provide a unique mapping of multivariate data to 2-D without any loss of information. Using this methodology, some defects were found that were actually "beneficial" and in small quantities improved the yield and speed performance (access time) of the wafer. While using conventional methods, the yield on the wafers couldn't be improved beyond a plateau and hence had led the engineers to think of redisgning

the chip, the process window discovered using the Parallel Coordinate methodology provided some insights that helped in improving the yield of the process significantly. This technique is extremely useful in yield analysis and improvement, process control and design of experiments.

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