Tuesday Morning, November 3, 1998

Manufacturing Science and Technology Group
Room 317 - Session MS-TuM

Overview: Integration for Manufacturing

Moderator: J.J. Sullivan, MKS Instruments, Inc.

8:20am **MS-TuM1 Reaction/Annealing Pathways for Forming Ultrathin Silicon Nitride Films for Composite Oxide-Nitride Gate Dielectrics with Nitrided Crystalline Silicon-Dielectric Interfaces for Application in Advanced CMOS Devices**, ***G. Lucovsky***, North Carolina State University **INVITED**

Aggressive scaling of CMOS devices requires gate dielectrics with oxide equivalent thicknesses of ~1 nm by 2012. Direct tunneling is a limitation in FETs when oxide thicknesses are reduced to <2 nm. In addition, boron diffusion from p+ poly-Si gate electrodes in PMOS FETs leads to additional electrical problems for oxide thicknesses <4 nm. Interfacial nitridation improves reliability in NMOS FETs; however, it is not effective in PMOS FETs due to of boron pile-up at the Si-dielectric interface. One solution to these problems is the integration of composite oxide-nitride composites with nitrided interfaces; NON dielectrics, into CMOS devices. The paper discusses: i) deposition of hydrogenated silicon nitride by remote plasma-enhanced chemical-vapor deposition (RPECVD); ii) characterization of plasma-deposited nitrides by IR and AES; and iii) effects of post-deposition annealing on the bonded-H content. Formation of nitride thin films for NON composite dielectrics requires two process steps: i) deposition of a hydrogenated silicon nitride film at 300°C by RPECVD, followed by ii) rapid thermal annealing in an inert ambient at 900°C. During the anneal H-atoms are evolved from near-neighbor SiH and SiNH bonds, and the resulting Si and N-atom dangling bonds combine to form new SiN bonds accounting for the device-quality electrical performance. Electrical performance of devices with composite i) oxide-nitride-oxide, ONO, dielectrics, and ii) ON dielectrics with fully nitrided interfaces, NON, is discussed. For example, we demonstrate that approximately 2 molecular layers of nitride, ~0.8 nm, at the top surface of the NON dielectric is sufficient to stop B-penetration out of p+ poly-Si gate electrodes during dopant drive-in/activation anneals. Finally, nitrides produced by the two step process are qualitatively different from CVD nitrides deposited at higher temperatures, ~500°C, and subjected to post-deposition anneals in oxidizing ambients.

9:00am **MS-TuM3 Process Mixing in Cluster Tools**, ***R.A. Powell***, Novellus Systems **INVITED**

Cluster tools are widely used in advanced microelectronic manufacturing because they offer high productivity and the ability to improve thin film and interface quality through vacuum-integrated processing. While such tools are often dedicated to a single technology such as plasma etching, PVD, or CVD, it is common to integrate a number of different process technologies within the same tool. For example, the integrated process sequence of wafer degas+ preclean + PVD Ti + PVD TiN + PVD AlCu + PVD TiN can be carried out in a PVD cluster tool without a vacuum break to deposit an AlCu interconnect line. Understanding and managing the interplay between successive steps is critical to successful process integration-which in turn has an important effect on tool performance, productivity and cost of ownership. Looking forward, there is growing interest in clustering fundamentally different deposition methods such as PVD and CVD onto a common wafer handling platform to take advantage of their complementary benefits. This talk will discuss the motivation and challenge of integrating these and other processes on advanced cluster tools with a focus on film deposition. Generic issues of mixing and matching different processes on a cluster platform will be discussed with regard to vacuum requirements, ambient purity, thermal cross-contamination, and the choice of single wafer versus batch processing. Specific examples from both PVD and CVD cluster tools will be used to illustrate the general points made.

9:40am **MS-TuM5 Process Integration Overview: Development and High Volume Manufacturing of Microprocessor Products**, ***R.A. Gasser, Jr***, Intel Corporation **INVITED**

Intel Corporation provides ~80% of worldwide demand for microprocessors. Continuing to meet this demand requires the development of high performance microprocessors using the most advanced process technology available. Meeting this demand also requires the ability to ramp the technology at high volumes in many factories at the same time. This talk will first present an overview of the economics of microprocessor manufacturing. This overview will show why it is imperative for the key participants in this industry to be able to consistently deliver both high levels of transistor performance and process integration using the most advanced equipment available. Next, there will be a review of methods for robust process design. Robust process design is key to laying the foundation for eventual process ramp. Finally, there will be an overview of methods for ramping the process technology to very high volumes, while achieving high product yields.

10:20am **MS-TuM7 Value Chain Integration**, ***P.S. Peercy***, SEMI/SEMATECH **INVITED**

Driven by continuously increasing competitive pressures from increasing globalization, the semiconductor industry has undergone major structural changes over the past few years. As recently as the early 1980s, most of the process and fabrication research and development was performed primarily in large vertically integrated companies in the industry. Mission-driven research in the central research labs and the R&D pilot lines of these companies yielded most of the technology required to keep the industry's productivity growing exponentially at a rate of 25-30% per year. Today, the semiconductor industry in the U.S. has largely stratified into systems companies, device manufacturing companies, and equipment, subsystem, component, and materials suppliers. In addition, competitive pressures and changing business conditions have shifted the focus of much of the research in the central research labs of the device companies away from fabrication equipment and processing technology. As a result, an increasing amount of the new processing equipment, process technology, and materials development comes from the supply chain today. Tomorrow, the suppliers will be expected to provide virtually all of the new processing equipment and technology required by the device manufacturing sector of the industry. With the increasing stratification of the supply chain, increased vertical communication and coordination is necessary. The efficiency of the supply chain, and the industry, can be greatly increased by close customer-supplier alliances at all levels in the supply chain. Such "value chain integration" can provide a common language for simultaneous communication of requirements to all levels of suppliers. Further, joint development of the technology permits optimization of the research and development efforts throughout the supply chain. It permits competitors to cooperatively perform the research for generic, pre-competitive technologies required for the continued advancement the technology. Additional optimization comes from relying on the expertise of suppliers at all levels in the supply chain; if the requirements are developed jointly, the expertise of suppliers of a given component or subsystem frequently permits redesign and implementation in a more cost-effective and reliable manner. We will examine value chain integration in general with examples of the benefits realized through true customer-supplier alliances, then examine application of value chain integration to the semiconductor industry.

11:00am **MS-TuM9 Factory Integration in the NTRS: Future Factory Level Issues and Needs**, ***G.M. Gettel***, SEMATECH / Texas Instruments, Inc. **INVITED**

The global challenge in the National Technology Roadmap for Semiconductors (NTRS) is to keep the semiconductor industry's productivity engine on track by staying on the 25-30% per year manufacturing cost reduction curve. The industry has been successful in the past in driving down the curve by using feature size reductions and wafer diameter increases. In the future, these two approaches will continue to be exploited but four factory level challenges will have to be addressed to keep the industry from getting derailed. The four challenges are: Escalating factory cost; Factory investment risk and time factors; Overall Factory Effectiveness; and Process / Factory complexity. Factory capital costs are escalating over time up an exponential curve. With the escalating factory costs comes escalating investment risk. Future factories will need faster design, construction, tool installation and ramp in order to pay back in a reasonable time period. Improved bottleneck and average tool OEE are needed. In the future, incoming equipment in an operation will need to have a higher initial OEE and reach maturity quicker. Processes (driven by smaller feature sizes and larger wafer diameters) and factories (driven by economy of scale) will be increasingly complex in the future. This complexity is increasing exponentially. The systems capability to deal with the complexity is evolving at a slower pace resulting in a "data overload gap". These factors drive the need for improved decision support capability. Future factories will require more tool to tool automation, better wafer and die traceability and improved material control systems. Software content in equipment is growing by more than 25% per year. To prevent this increased amount of software complexity from derailing effective factory operation, more reliable and predictable software will be

required. This presentation will review the trends, issues and potential solutions for these four difficult factory level challenges.

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