Manufacturing Science and Technology Group
Room 317 - Session MS-TuA

Process, Integration, and Modeling
Moderator: K. Aitchison, Novellus Systems

2:00pm **MS-TuA1 Pattern/Etch/Clean Process Interactions for 0.18um CMOS Gate Formation***, **R.J. Gale**, R. Kraft, R.T. Laaksonen, A.L.P. Rotondaro,* Texas Instruments **INVITED**

As device dimensions continue to shrink to 0.18um and below, the interaction between steps in a process flow becomes more critical. These interactions can be synergistic. In many cases, however, the processes must be co-optimized to minimize the negative effects. One of the most critical process modules in a CMOS device flow is the formation of the gate geometry. We will focus on pattern, etch, and post-etch clean interactions in forming the gate. Dry etch is used to reduce the photoresist patterned line width. This approach permits the wafer patterning to be performed in a more robust process regime thus producing less variation. Once the desired line width reduction has been accomplished, the polysilicon is dry etched, stopping on the thin (<30A) gate oxide. Finally, the remaining photoresist and etch polymer residues must be removed without stripping the thin gate oxide protecting the active regions of the device. Changes in the dry etch process to maximize anisotropy to provide vertical profiles for the gate geometry and high selectivity to gate oxide drive a more aggressive post etch clean process that also must be optimized for oxide selectivity and critical dimension control. This paper discusses the challenges and tradeoffs to successfully accomplish the 0.18um gate formation.

2:40pm **MS-TuA3 Dual Damascene : Etching Process Characterisation of "Self Aligned" and "Counter Bore" Architectures***, **P. Berruyer**, F. Vinet,* LETI-GRESSI, France*; H. Feldis,* SGS-Thomson, France*; E. Tabouret, Y. Trouillet,* LETI-GRESSI, France*; Y. Morand,* SGS-Thomson, France

One of the main challenges of the next few years is the improvement of interconnect performances, namely integration density and dynamic performances. This can not be done without combining improvement in both design and technology. In term of technology, different ways are explored : introduction of low k dielectric and low resistivity metal. Concerning low resistivity metal, copper seems to be the best candidate to replace AlCu. But the main disadvantage of this material is its high resistance to plasma etching. Taking into account that copper is highly resistant to plasma etching, that Chemical Mechanical Polishing processes are available and that dual damascene architecture can significantly increase interconnect density, copper is usually introduced in a damascene architecture. Among the different ways of achieving dual damascene structures, two of them, called " self aligned " and " counter bore " have to be taken into account. In this paper we will first describe the process steps of these two architectures. We will point out that both architectures require the development of a specific high aspect ratio dielectric etching process with high selectivity to nitride. A medium density reactor (TEL Unity DRM) will be used for the experiments. Different process conditions will be applied to dual damascene structures for a morphological characterisation. Major attention will be paid on selectivity to nitride, microloading, etch stop and CD control. Etch rate and selectivity to photoresist will also be studied. The architectures and the etching processes will be compared on an electrical lot with copper metallisation. Contact resistance and yield on 10 million contact chains will be measured. The advantage and drawbacks of each architecture will be discussed with regard to etching processes. An optimised dual damascene process will be proposed.

3:00pm **MS-TuA4 Low k Polymer Etching for Dual Damascene Technology Application to SILK Material***, **F. Vinet**, E. Tabouret,* LETI-GRESSI, France*; Ch. Vivensang,* Tokyo Electron Europe LTD, France

Scaling down of interconnect requires a change in architecture and materials to be integrated. Dual Damascene scheme in combination with copper as metal conductor, appears to be the most acurate choice for sub 0.18 µm design rule technology. The dielectric material necessary for this application is still under improvement to achieve the required properties such as, dielectric constant<2, thermal stability and good adhesion on mineral or organic layers. The most advanced materials are based on polymers. In order to etch these materials, a hard mask is necessary due to their poor resist selectivity (1:1).Silicon dioxide (SiO2)is the most commonly used hard. Depending on the polymer composition, the compromise between high aspect ratio and mask erosion has to be found. Among the different available materials, SILK from Dow Chemicals, presents a chemical stability compatible with the thermal budget of our current technology. Moreover, this material is purely organic and contents no silicon; in this case an etching chemistry without fluorine can be used, ensuring a good selectivity to the hard mask. The etching properties, as well as the requirements related to the use of a Dual Damascene architecture have been investigated in this paper. A 1500Å thick SiO2 hard mask was deposited on top of 1µm spin coated SILK. By using DUV lithography 0.225 µm holes and 0.3/0.3 µm L/S patterns were defined. A medium density etcher from TEL, DRM85 UnityII was used for the experiments. By using a pure O2 chemistry, an overhang between hard mask and SILK is observed ; moreover due to isotropic etching, the sidewalls after etching are bowed. In order to overcome these effects, different chemistries have been tested in combination with etching process parameters to form a passivating layer. With optimised conditions, 0.225 µm holes were obtained with straight profiles. In our experiments, the limitation for higher aspect ratios is due to lithography and not to etching conditions. Whatever the Dual Damascene structure is used, successive steps of fluorinated and non fluorinated chemistry has to be used to etch alternatively SiO2/SILK/ SiO2.The effect of such a sequence has been studied on the etched profiles as well as the influence of reactor fluorine memory effect. Optimised conditions for both, process and reactor, are proposed to ensure a reliable process for sub 0.18µm technology.

3:20pm **MS-TuA5 Manufacturing Issues for MEMS Production***, **K.W. Markus**,* MCNC **INVITED**

As the commercial and military implementation of MEMS technology solutions moves further up the line from research to consumer and commodity applications, the need for a robust manufacturing technology base for MEMS continues to increase. MEMS, the merging of computation with sensing and actuation into an integrated system-based solution for problems pertaining to the physical world, has benefited greatly and grown rapidly out of the widespread infrastructure developed in the U.S. for the manufacture of integrated circuits (IC). The U.S. approach to MEMS applies the repetitive layering, batch-processed wafer methods of the integrated silicon circuit manufacturing industry to achieve revolutionary strides in mechanical miniaturization and system integration. This outgrowth from the IC industry has both benefits and pitfalls, and it is going to be capitalizing on the benefits and navigating the pitfalls that will determine the success of the transition of MEMS from its current low or sporadic volumes to the high-volume successes that will demand large-scale production capabilities. One of the many benefits that MEMS derives from its common base with the IC industry is the methodology behind its fabrication sequences. Most MEMS processes can be decomposed to a repeating series of material deposition, patterning and subsequent removal of specific areas of the material. This layering is repeated until the basic structure is created either on or within the silicon wafer. While many of these steps, or unit processes, are similar to those used in IC processing, the mechanical nature of MEMS puts additional stringent requirements on the processes that do not exist in the IC processes. Beyond the fabrication of the basic wafer structure, the releasing of the structures, the handling of these released wafers or die, the packaging, and the testing of the MEMS devices all can challenge even the most sophisticated and technically advanced manufacturing line. While there is a strong and vibrant manufacturing infrastructure for the IC industry, the uniqueness of some of the key steps of MEMS technology challenge the existing manufacturing technology infrastructure and place challenges and potential limitations on the development of a comparable support-structure for MEMS. Much of the IC industries infrastructure has grown as a result of, and not in advance of, the explosive growth the IC industry in the last 15 years. While the outlook for MEMS is quite strong ($9B - $30B by 2000)@footnote 1@ , it is a mere trifle when compared against the $148B@footnote 2@ (1995) IC market (year 2000 projection $371B) . MEMS will need to find creative and unique ways to ensure that the level of attention necessary to help drive the growth of manufacturing infrastructure are found and nurtured, despite the overwhelming shadow of the IC market. This presentation will discuss the manufacturing issues affecting the growth of MEMS from commercial curiosity to manufacturing reality, including design and simulation tools, fabrication equipment, through-put and resources, packaging, testing and reliability. @FootnoteText@ @footnote 1@ Micromachine Devices newsletter, August 1997 @footnote 2@ World-wide Merchant Semiconductor Forecast, Source: ICE, Status 1996

4:00pm **MS-TuA7 Design of a 300 mm CVD Tungsten Reactor using Computational Fluid Dynamics**, ***E.J. McInerney***, *T.M. Pratt, A. Tahari,* Novellus Systems

Over the next several years, the semiconductor industry will transition to 300 mm wafers for IC fabrication. To support this shift, the semiconductor equipment companies must develop 300 mm processing tools that are both manufacturing worthy and cost effective. In the past, designing equipment for larger sizes was primarily a matter of scaling the components: chamber, showerheads, heaters, etc. For batch systems, often the batch size would also be reduced to minimize the gain in footprint. However, as capital equipment costs become an increasing fraction of wafer fabrication costs, it becomes necessary for semiconductor equipment to not only handle larger sizes, but also to be substantially more cost effective. We report here on how computational fluid dynamics modeling was used to guide the design and development of a high throughput, 300 mm multi-station CVD tungsten reactor. Through modeling we were able to investigate novel gas-based isolation schemes that allowed the individual deposition stations to run separate processes, without cross contamination. The resulting reactor can simultaneously deposit silane reduced and hydrogen reduced tungsten films at adjacent deposition stations without the danger of gas phase nucleation or WF@sub 6@ device attack. This leads is a significant drop in the idle time of deposition stations and a large boost in throughput.

4:20pm **MS-TuA8 Computational Flow Modeling for Electrostatic Chuck Applications**, ***L.A. Gochberg***, Novellus Systems, Inc.

An electrostatic chuck used in a deposition or etching process is comprised of a ceramic material with an embedded electrode, on which a wafer is placed in the reactor chamber. The gas flow paths on the backside of the wafer can be adjusted to help control the wafer temperature. The dimensions of these flow pathways can be as small several microns, and at typical backside gas operating pressures (1-10 Torr), the flow can be anywhere between continuum and free molecular flow. Though tools are available to model these flows (Direct Simulation Monte Carlo and Navier-Stokes with slip boundary conditions), these flow conditions, typical in wafer processes, bring up some significant computational challenges. Also, the 3D nature of the real chuck flow with all its complex geometry compounds the numerical difficulties. In this paper, the focus will on a 2D approximation to the flow on the backside of the wafer, which is essentially flow between two flat, parallel circular disks. This geometry is quite similar to the 3D geometry in the electrostatic chuck, but without the complex set of gas grooves. Computations will be performed using Navier-Stokes computational fluid dynamics (CFD) with and without slip boundary conditions, Direct Simulation Monte Carlo (DSMC), and an analytical solution to the problem. These results will be compared to experimental data for helium gas flow through that same geometry. Comparisons show an excellent agreement between all the computations and the experiments in the continuum and near-continuum transition flow regime. The DSMC results and analytical solution match well with the data throughout all the flow regimes. However, the CFD with slip shows a capability in this 2D geometry to capture the trends seen in the data and DSMC out to much higher Knudsen numbers than would be typically expected. These CFD with slip results can be used as a design tool to conservatively estimate backside gas pressure distributions and reliably design gas distribution channels.

4:40pm **MS-TuA9 TEOS CVD Topography Simulation Using Surface CHEMKIN and EVOLVE**, ***A.H. Labun***, Digital Equipment Corporation; *T.S. Cale,* Rensselaer Polytechnic Institute; *P. Ho, H.K. Moffat, M.E. Coltrin,* Sandia National Laboratories

Although the pyrolysis of Si(OC@sub 2@H@sub 5@)@sub 4@ (TEOS) leads to formation of a highly reactive deposition precursor, increasing the residence time in a chemical vapour deposition (CVD) process leads to more, not less, conformal SiO@sub 2@ deposition in high aspect ratio features, contrary to the assumption of a first order deposition reaction commonly used in topography simulation. A newly developed Surface CHEMKIN interface in the EVOLVE 5.0 topography simulator allows EVOLVE to be used in conjunction with CHEMKIN-based reactor codes to explore this and other CVD reaction mechanisms and make process recommendations. Ab initio calculations and experiments lead to consideration of a network of 8 reversible, heterogeneous reactions and 3 reversible, homogeneous reactions, involving 5 surface species and 6 gasses. Under short reactor residence time conditions relatively little TEOS decomposes and it remains the dominant constituent of the bulk gas, but transport limitations cause byproduct gasses to dominate in submicron features. They promote the reverse heterogeneous reactions, slowing the deposition rate inside the features and causing nonconformal films. The sticking coefficients of TEOS and the precursor may vary substantially over the topography and during the deposition. Decomposition of the TEOS under longer reactor residence time conditions leads to similar gas compositions inside and out of the features and hence film deposition in the features becomes conformal.

5:00pm **MS-TuA10 Plasma-Induced Nitridation of the Gate Oxide Dielectrics: Linked Equipment-Feature-Atomic Scale Simulations**, ***V. Sukharev***, *S. Aronowitz, H. Puchner, V. Zubkov, J. Haywood, J. Kimball,* LSI Logic Corporation

Quantum chemical calculations were employed to get insight into the mechanisms involved in plasma-induced nitridation of gate oxide that will suppress boron penetration. The roles played by the nitrogen cations and atoms were explored. Based on these results, we assumed the following model for the nitrogen incorporation: nitrogen cations cleave bonds in substrate subsurface region; the depth of the damaged layer is determined mainly by the energy of the incident ion, binding energy of nitridated material and its density. Nitrogen atoms, whose concentration is usually several orders of magnitude greater than the cation concentrations, readily react with dangling bonds to produce @>=@Si-N- and @>=@Si-O-N- radicals. A subsequent anneal produces an appropriate condition for reaction between the above radicals and results in the nitrogen insertion into the SiO@sub 2@ ring structure. Thus the nitrogen cations play the role of the promoter for the entire SiO@sub 2@ nitridation. It was shown that B interaction with siloxane rings that contain incorporated nitrogen yielded a larger energy gain than rings without nitrogen. This explains the chemical nature of the nitrogen-induced barrier effect. Monte Carlo (PROMIS) simulations were used to simulate the necessary energy of incident N@sub 2@@super +@ cations to produce the bond cleavage down to a particular depth in the amorphous SiO@sub 2@ layer. A combination of the Hybrid Plasma Equipment Model and Plasma Chemistry Monte Carlo Simulation codes were used to simulate nitrogen atomic and cation fluxes and their angular and energy distributions at the wafer surface. Combining simulated cation energies with PROMIS Monte Carlo simulation results make it possible to derive the plasma process parameters that will permit a desired level of nitridation to be reached.

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