## Manufacturing Science and Technology Group
## Room 317 - Session MS-MoA

### Contamination Free Manufacturing

**Moderator:** A.C. Diebold, Sematech

2:00pm **MS-MoA1 Green House Effect and LSI Process Technology**, ***K. Okumura***, *T. Ohiwa,* Toshiba Corporation, Japan **INVITED**

While LSI devices contribute to saving energy, their fabrication consumes large amounts of electric power and PFC gases. This paper will discuss the new LSI process technology to alleviate such negative aspects. Among the process tools, especially the furnaces and dry pumps consume a large quantity of electric power. The fast temperature processor (FTP), which realizes ramp temperature up and down at high speed, succeeds in maintaining temperature at 300 - 400 °C and ramping up to 800 - 900 °C only when processing. This leads to a 30 - 50 % power reduction compared to the conventional furnace which constantly maintains its temperature at 800 - 900 °C. Dry pumps with an inverter controlled DC motor drive consume half as much power as conventional induction motor drive systems. Furthermore, quick response of the DC motor without over-current makes it possible to turn it on only when necessary and off during machine idling, which leads to 15 - 80 % less power. In RIE and CVD machines, as much as 10 - 15 SLM of purge N@sub 2@ gas is used in order to prevent clogging of dry pumps by by-products. Pure N@sub 2@ gas generation also requires a vast amount of electric power. Therefore, reduction of N@sub 2@ gas is another effective approach. A dual in-line cold trap was newly developed for this. It consists of two traps. One traps by-products before the dry pump, and the other can be flashed meanwhile. Improving the efficiency of gas usage leads to reduction of PFC consumption. A new gas circulation system was developed, which pumps the exhausted gas still containing usable process gas into the RIE reaction chamber to be reused. Because many kinds of PFC gases after plasma processing eventually change to the most stable CF@sub 4@ gas, recycling of CF@sub 4@ gas is a key point. We have developed a dual trap system which operates at liquid N@sub 2@ temperature. It is capable of trapping CF@sub 4@ gas exhausted from an RIE reaction chamber. This system has the possibility of distillation of PFC gas by the appropriate control of regeneration temperature.

2:40pm **MS-MoA3 Ultra-Low-Temperature Growth of High-Integrity Silicon Oxide and Nitride Films by High-Density Plasma with Low Bombardment Energy**, ***K. Sekine***, *R. Kaihara, Y. Saito, M. Hirayama, T. Ohmi,* Tohoku University, Japan

As semiconductor devices are scaled down to smaller dimensions, conventional processing temperature such as 900°C will be incompatible with the desired device structure. For example, conventional high-temperature gate insulator formation process changes the impurity profile previously formed in the substrate. Moreover, it is necessary to introduce metal substrate SOI device for future high speed (>1GHz) ULSI device. To realize the metal substrate SOI device, all of manufacturing processes have to be done at below 550°C. Thus gate insulator also must be formed below 550°C. Therefore lowering growth temperature of high-integrity gate insulator is a key for future metal substrate SOI device fabrication. High integrity ultra-thin silicon oxide and nitride films can be obtained at 430°C by direct oxidation and nitridation of silicon surface. Such a low temperature oxidation and nitridation could be realized by employing newly developed high-densit!y plasma system with low ion bombardment energy less than 7eV and high plasma density above 10@super12@cm@super-3@. The electrical properties of these films are nearly the same level as those of thermally grown films. This technology becomes very promising for fabricating feature metal substrate SOI devices and silicon nitride gate MISFET.

3:00pm **MS-MoA4 Low-Temperature Large-Grain As-Deposited Poly-Si Formation by Microwave-Excited PECVD Using SiH@sub 4@/Xe**, ***W. Shindo***, *S. Sakai, T. Ohmi,* Tohoku University, Japan

We have achieved as-deposited large-grain polycrystalline silicon at a temperature of 300°C by plasma enhanced CVD using SiH@sub 4@/Xe. The grain size evaluated by X-ray diffraction is 25nm, which is believed to be the largest grain size among 100nm-thick as-deposited poly-Si films fabricated by various methods at low temperature. High-density (>10@super 12@cm@super -3@) plasma having very low electron temperature (approximately 1eV) excited by microwave irradiation was used for the film growth. Plasma density and electron temperature dominate ion flux density and ion kinetic energy incident on the substrate surface, respectively. Thus, high-flux and low-energy ion bombardment (

3:20pm **MS-MoA5 Balanced Electron Drift Magnerton Plasma Source for Uniform SiO@sub 2@ Etching**, ***R. Kaihara***, *T. Ohmi,* Tohoku University, Japan*; H. Komeda,* Sharp Corp., Japan*; Y. Hirayama,* Tokyo Electron Yamanashi Ltd., Japan*; M. Hirayama,* Tohoku University, Japan

Magnetron etcher using dipole ring magnet has demonstrated its high selectivity with lower micro-loading effects. When parallel magnetic field is applied by dipole ring magnet, the uniformity V@sub dc@ and ion flux is degraded by ExB drift of secondary electrons on the wafer. The inherent non-uniformity causes crucial problems such a charge up damage and etching non-uniformity. In order to improve non-uniformity of V@sub DC@, gradient magnetic field has been employed in a magnetron etcher using dipole ring magnet. Almost uniform V@sub DC@ profile can be achieved by optimizing the magnetic field profile. Even though optimizing magnetic field profile is effective, there is some problems such as restricted process window and non-uniformity of ion flux. On the other hand, we applied RF(100MHz) to upper annular electrode in order to improve non-uniformity of V@sub DC@ and ion flux. The electron drifts can be balanced between the upper annular electrode and the lower electrode. Uniformity of V@sub DC@ (±4V) and ion flux (±3%) are simultaneously obtained by the balanced electron drift (BED) magnetron etcher. Excellent etching profile of 0.15µm contact hole is also obtained uniformly on 200mm wafer.

3:40pm **MS-MoA6 Influence of Wafer Back Surface Finish on Dry Etching Characteristics**, ***S. Muramatsu***, *K. Ando, H. Nanbu, H. Miyamoto, T. Kitano,* NEC Corporation, Japan

Process tolerance and controllability have become more severe with the scaling down and integration of devices. Wafer back surface finish is a factor affecting the process conditions such as dry etching and rapid thermal annealing. In this study, the correlation between back surface roughness and dry etching characteristics was investigated. The back surface roughness was changed from Ra=0.41 nm to 50.1 nm by final back surface treatments (mechanochemical polishing or chemical etching). Contact-hole etching with CHF@sub 3@ gas was performed for interlayer CVD oxide deposited on the front surface of wafers. The etching rate for a smooth back surface (0.41 nm) was increased by 1.1 times over that for a rough back surface (50.1 nm). During contact-hole etching, the wafer temperature of the smooth back surface was10°C lower than that for the rough back surface. This is due to the difference in electrostatic chucking (Ra=80-120nm) force during contact-hole etching. When the smooth back surface wafer was used, the adhesion area between the dry-etching stage and the wafer back surface increased because the back surface roughness was small. Consequently, the wafer can be cooled down sufficiently and the etching rate dominated by gas absorption was increased. As well as the etching rate, the position where residual gas was deposited inside the contact hole was governed by the degree of the wafer back surface finish. These experimental results indicate that the roughness of the wafer back surface should be well controlled for fabricating advanced devices.

4:00pm **MS-MoA7 Precise Control of Gas Ratio in Process Chamber**, ***Y. Shirai***, *O. Nakamura,* Tohoku University, Japan*; N. Ikeda, R. Dohi,* Fujikin Inc., Japan*; T. Ohmi,* Tohoku University, Japan

In 300mm wafer generation, many kinds of single wafer processing will be necessary to establish higher process uniformity on a wafer. For achieving low cost production, it is necessary high-rate processing such as wafer/min including load-unload time. Process gas distribution system is one of the most critical issues for process uniformity and high-rate processing. Especially, high quality and uniformity of film formation process strongly depends on initial gas distribution in a process chamber. We have developed advanced integrated gas system and studied process gas ratio in process chamber using FT-IR method. We have prepared two types of integrated gas distribution system. One is the conventional system consists of MFC and air operate valve, the other is the advanced system consists of new pressure flow controller with electric valve. This new pressure flow controller built on the principle that the flow rate is directly proportional to the upstream pressure if the upstream pressure is more than two times of downstream pressure. We have introduced three kinds of process gases into a process chamber. The conventional system shows over shoot phenomena. The process gas concentration increase more than two times of the steady state. In addition, it takes more than 20 seconds to be steady state of gas ratio and chamber pressure after the valve operation. On the other hand, the advanced system does not show over shoot phenomena. The steady state of gas ratio and chamber pressure can be obtained within 2 seconds after the valve operation.

4:20pm **MS-MoA8 Clean Aluminum Oxide Formation on Surface of Aluminum Cylinder in an Ultraclean Gas Sampling System**, ***Y. Ishihara***, *N. Itou, T. Kimijima, T. Hirano,* NIPPON SANSO Corporation, Japan

Because it is difficult to obtain enough space for a gas-analysis system in semiconductor manufacturing lines, gas purity is usually confirmed by an ex-situ analysis of gas sampled inside the gas-sampling cylinder (sampler). In order to analyze a trace impurities, it is necessary to significantly reduce the contaminants generated in sampler and to fabricate a surface and/or material with an extremely low outgassing rate. We have produced a sampler made of pure Al produced during plasma oxidation in 3% O@sub 2@/Ar after the EX process.@footnote 1@ Nevertheless, the H@sub 2@ concentration in N@sub 2@ or Ar sealed at 0.58MPa in the sampler increased from below 1ppb to 8ppb after 168hours. The CO and CO@sub 2@ concentration in O@sub 2@ also increased. Wet cleaning was carried out in the sampler in the plasma oxidation state by DI water for 72hours at a flow rate of 2L/min. After wet cleaning, the sampler was annealed at 423K for 72 hours in N@sub 2@ without exposure to air. We have confirmed that amorphous @gamma@-Al@sub 2@O@sub 3@ film with a thickness over 0.5μm was formed on the inner surface of the sampler using cross-sectional TEM observation. We have observed that the H@sub 2@ concentration in Ar or N@sub 2@ was maintained below 1ppb, the detection limit of the GC, for 168hours. The CO and CO@sub 2@ concentration in O@sub 2@ were also sufficiently low. These results suggest that the amorphous @gamma@-Al@sub 2@O@sub 3@ film formed by a series of treatments as already mentioned function as a gas-barrier film with an anti-catalytic property. @FootnoteText@ @footnote 1@H. Ishimaru, J.Vac.Sci.Tech., A7(3) 2439 (1989)

4:40pm **MS-MoA9 Gradational Lead Screw Pump Development**, ***K. Ando***, T.D.Giken Co., Ltd., Japan*; I. Akutsu,* DIAVAC Limited, Japan*; T. Ohmi,* Tohoku University, Japan

Because the silicone device industry is innovating their production processes toward the larger wafer size and the higher process speed, a vacuum pump is required higher pumping speed through ranges of the both viscous and molecular flow. There has been no known conventional pumps that have been developed so as to vacuum a chamber down to 0.01 Torr with stable exhaust velocity over the entire region including the molecular flow region. All of them provide stable pumping speed only down to 0.1 Torr. The "GLS Pump" unlike these conventional pumps demonstrated the high pumping capability of 0.0004 Torr and the pumping speed of 3600L/M over the viscous and molecular flow ranges. The improved performance is attributable to the GLS employed for the rotor design. The pump utilizes a small amount of oil. The mass analyzer test(max. mass number 120) revealed that there is no evidence of the reverse diffusion in the pressure range above 0.002 Torr with a small amount of N2gas injected. In summary, the GLS Pump has enough displacement and large intake conductance. Low reverse diffusion is in practical operation. The pumping speed is high. The power consumption is low. The byproduct is transferred and ejected from the exhaust port through the operation mechanism. The radical deposit is minimized if the case temperature is maintained at 150°C. Although manufacturing this pump requires high level of skill, the pump structure is rather simple and the maintenance is easy hence it will increase the mean time between maintenance and reduce the maintenance cost. The detail report will be prepared on the characteristics of the GLS, the pump structure, and the performance attributes.

5:00pm **MS-MoA10 Etching and Cleaning of Silicon Wafers using HF Vapor Process in the Non-Condensed Etching Regime**, ***Y.-P. Han***, *H. Sawin,* Massachusetts Institute of Technology

We have studied oxide etching mechanisms of HF vapor etching process in two regimes: the condensed regime (liquid phase) and the non-condensed regime (gas phase). In the condensed regime, the etching rate of oxide is greatly affected by the flow rate of the reactant stream and the total pressure of reactor, which can change the mass transfer rates of both reactants and products. The rate limiting steps of the etch rate have been studied at various conditions by changing the temperature of the reactor, the partial pressure of the reactants and the flow rate. The etching rate of oxide in the non-condensed regime was mainly limited by the surface reaction rate at higher temperature, but the mass transfer rate became more important at lower temperature. We also have investigated the cleaning of Na from silicon wafer in HF vapor process. It was observed that Na contamination on thick thermal oxide films was typically removed by HF vapor process. On thinner oxide films, i.e. 1-2 nm native oxide, only part of the contaminated Na was typically removed by this process. The addition of SiF4 to the HF/H2O process, i.e. HF/H2O/SiF4 was found to improve the cleaning efficiency of Na from silicon surfaces. The volatile product is believed to be Na-OSiF3.

# Author Index

## Bold page numbers indicate presenter