Electronic Materials and Processing Division
Room 314/315 - Session EM1-ThA

Dielectrics
Moderator: E. Garfunkel, Rutgers University

2:00pm **EM1-ThA1 Short Range Order and Electronic Structure of Amorphous Silicon Oxinitride**, ***V.A. Gritsenko,*** Siberian Branch of Russian Academy of Science, Russia; *R.W.M. Kwok, Y.H. Ng, J.B. Xu,* The Chinese University of Hong Kong, China; *I.H. Wilson,* The Chinese University of Hong Kong, Hong Kong

The short range order and electronic properties (electronic structure, energy diagram, and charge transport) of bulk amorphous silicon oxynitride (a-SiO@sub x@N@sub y@) were reviewed for the further understand of a-SiO@sub x@N@sub y@ the properties of gate oxynitride of MOS devices on the atomic scale. Amorphous SiO@sub x@N@sub y@ consists of Si-O and Si-N bonds and involves five types of tetrahedra: SiO@sub@nu@@N@sub 4-@nu@@ for @nu@ = 0, 1, 2, 3, 4. The local bonding in SiO@sub x@N@sub y@ is governed by the Mott rule as shown in the equation 4=2x+3y. From x-ray photoelectron spectroscopy, ultraviolet photoelectron spectroscopy, x-ray emission spectroscopy and the simulation of the electronic structure, we concluded that Si-O bonds in a-SiO@sub x@N@sub y@ are created by O 2s, 2p and Si 3s, 3p, 3d bonding states, and Si-N bonds are created by N 2s, 2p and Si 3s, 3p, 3d bonding states. Barriers for electron and hole injection at Si-SiO@sub x@N@sub y@ interface also gradually change with composition. The nature of the removal of hole traps from the SiO@sub 2@/Si interface during oxide nitridation was understood from the removing of Si-Si defects. The origin of Si-Si bond creation near the top surface of gate oxynitride after re-oxidation are understood on the basis of the Mott rule through the oxidation of nitride species Si@sub 3@N to form Si-Si bonds.

2:20pm **EM1-ThA2 Cathodoluminescence Spectroscopy of Nitrided Si-SiO@sub 2@ Interfaces**, ***R. Bandhu,*** *J. Schäfer, A.P. Young, L.J. Brillson,* The Ohio State University; *H. Niimi, G. Lucovsky,* North Carolina State University

We use cathodoluminescence spectroscopy (CLS) to probe the electronic states at ultrathin gate dielectrics with nitrided Si-SiO@sub 2@ interfaces, known to improve reliability in advanced CMOS devices. The 5 nm-thick oxide at plasma-processed interfaces were: i) as-deposited (at 300 °C) structures, ii) 400 °C 30 min post-metallization annealed (PMA) in H2/N2, iii) 30 s 900°C rapid thermal annealed (RTA) in argon, and iv) a combination of both anneals. CLS emission energies and relative intensities vs. excitation energy (0.6-4.5 keV) were essentially unchanged for the as-deposited interface as reported for non-nitrided plasma-processed interfaces.@footnote 1@ In the near-IR (Ge detector), peaks appear at 0.8 and 1.0 eV, with the 1.0 eV peak intensity increasing with increasing electron energy. In the visible and near-UV (S-20 photocathode), features were observed at 1.9, 2.7 and 3.4 eV. From the depth variations, the 2.7 eV peak is generated near the surface of the oxide film, the 3.4 eV peak arises from the Si substrate, and the 1.9 eV feature comes from the near-interface region. After the PMA, CLS is essentially the same as for non-nitrided interfaces, except for an increase of the relative intensity of the 1.9 eV feature; after the RTA, analogous spectral features appear. However, the combination of the RTA and PMA does not completely suppress the 1.9 eV feature as for non-nitrided interfaces. CLS for as-deposited structures parallels optical second harmonic generation (OSHG); there are no differences with and without nitridation. However, as with OSHG, after the combined RTA/PMA, CLS reveals a substantial difference between nitrided and non-nitrided interfaces. The behaviors of the CLS features clearly distinguishes between interfacial defects (0.8 and 1.0 eV) and bulk defects (2.7 eV) which are significantly reduced by the combined RTA/PMA, and features that are intrinsic to the bonding chemistry, such as the 1.9 eV nitrided interface feature and the 3.4 eV Si substrate feature. @FootnoteText@ @footnote 1@A. P. Young, J. Schäfer, G. Jessen, R. Bandu, L. J. Brillson, H. Niimi, and G. Lucovsky, J. Vac. Sci. Technol. B, submitted. @footnote 2@G. Lucovsky, A. Banerjee, B. Hinds, C. Claflin, K. Koh and H. Yang, J. Vac. Sci. Technol. B15, 1074 (1997).

2:40pm **EM1-ThA3 Reliability of Ultra-thin Gate Dielectric formed with Nitrogen Implantation and Thermal Oxidation**, ***Y. Ma,*** *M.S. Carroll, F. Li,* Bell Laboratories, Lucent Technologies; *C.T. Liu,* Bell Laboratories, Lucent Technologies, US; *C.Y. Sung, M.M. Brown,* Bell Laboratories, Lucent Technologies

Traditionally nitrogen was incorporated into oxide through oxidation or post-oxidation annealing in N@Sub 2@O or NO. With a well engineered process, a thin layer of oxide containing nitrogen forms at SiO@Sub 2@/Si interface. The gate oxide reliability can be improved in terms of device lifetime. Recently, nitrogen incorporation with nitrogen implantation has been studied. In this paper, ultra-thin gate dielectric was thermally grown on nitrogen implanted silicon substrates. The advantages of this technique are (i) the oxide growth rate can be significantly suppressed and (ii) a multiple gate dielectric thickness on same chip can be realized. However, previous reports showed that gate oxide quality is degraded. In this paper, we demonstrated that higher thermal budget is needed to remove the implantation induced damage and to improve the gate oxide reliability. The gate oxides were either grown or post-oxidation annealed at higher temperature. We also will present that the gate oxide reliability are nitrogen dose dependent. Gate oxide quality was evaluated with three different techniques: current ramp breakdown, time dependent dielectric breakdown and hot carrier aging test. Both current ramp and TDDB indicate that the gate oxide was degraded with nitrogen implant. However, the hot carrier aging test showed that the device lifetimes were longer for the nitrogen implanted ones. CMOS transistors were also fabricated. Device performances such as channel mobility, drive current, device yield will also be reported.

3:00pm **EM1-ThA4 Effect of Substrate Temperature in SiO@sub x@N@sub y@ Films Deposited By Electron Cyclotron Resonance**, ***A. del Prado,*** *F.L. Martinez,* Universidad Complutense de Madrid, Spain; *M. Fernandez,* Instituto de Ciencia de Materiales, Spain; *I. Martil, G. Gonzalez Diaz,* Universidad Complutense de Madrid, Spain

High quality silicon oxynitride films for ULSI applications can be deposited at low temperatures using plasma assisted processes like the ECR-CVD technique.@footnote 1,2@ Physical properties of SiO@sub x@N@sub y@ films have been studied. The films have been deposited from mixtures of SiH@sub 4@, O@sub 2@ and N@sub 2@, using the ECR-CVD technique, with substrate temperature ranging from room temperature to 200°C. FTIR spectroscopy, AES and ellipsometric measurementes have been performed in order to characterize the films. Low bonded hydrogen content is observed along the entire composition range from Si@sub 3@N@sub 4@ to SiO@sub 2@. N-H bonds are present in all the films, while Si-H bonds are detected only for those films deposited under high SiH@sub 4@ partial pressure. No O-H bonds are detected. When substrate temperature is increased, a slight decrease in total bonded H concentration is observed. A small shift (7-20 cm@super -1@) in the main FTIR absorption peak (Si-N/Si-O stretching band) is detected. This behavior is attributed to hydrogen release from N-H bonds due to the substitution of H for Si, with no signicant change in the film composition. FWHM of the main FTIR peak decreases as temperature is increased for all the composition range, indicating an improvement in the film quality, as this parameter is related to the structural order of the film. Silicon oxide films (SiO@sub 2.0@) deposited at 200°C show improved properties with respect to those deposited at room temperature. FWHM decreases from 96 cm@super -1@ to 88 cm@super -1@, and shoulder-to-peak ratio from 0.30 to 0.25. The position of the Si-O stretching band (1072 cm@super -1@) is unaffected. These values are very close to those obtained for thermally grown oxides,@footnote 2@ while the thermal budget of the process is reduced. @FootnoteText@ @footnote 1@S. V. Hattangady, H. Niimi, G. Lucovsky. J. Vac. Sci. Tech. A 14 (6) 3017 (1996) @footnote 2@D. Landheer, Y. Tao, J. E. Hulse, T. Quance, D. -X. Xu. J. Electrochem. Soc. 143 (5) 1681 (1996)

3:20pm **EM1-ThA5 Roughness at Si/SiO@sub 2@ Interfaces and Silicon Oxidation**, ***X. Chen,*** Argonne National Laboratory; *J.M. Gibson,* University of Illinois, Urbana **INVITED**

Roughness at Si/SiO@sub 2@ interfaces and silicon oxidation With a plan-view transmission electron microscopy technique to directly image buried Si/SiO@sub 2@ interfaces, we studied the interface roughness resulting from the oxidation process. Our results show that thermal annealing in nitrogen at 900 C can dramatically remove the interface roughness for Si(100)/SiO@sub 2@ interfaces.(Xidong Chen and J. M. Gibson Appl. Phys. Lett. 70, 1462 (1997)) In contrast, Si(111)/SiO@sub 2@ interfaces, which tend to be smoother than Si(100)/SiO@sub 2@ interfaces, are not affected by annealing. A model to link interface roughness and silicon oxidation

kinetics was developed. This model not only qualitatively explains the difference between Si(111) and Si(100) interfaces that we saw but also shows that oxidation kinetics is the origin of the interface roughness. Hence, it might be a new approach to understand oxidation kinetics by studying interface roughness.

4:00pm **EM1-ThA7 Energy Dispersion of the Conduction Band Mass in Ultrathin SiO@sub 2@ Gate Oxides**, ***R. Ludeke,*** IBM T.J. Watson Research Center*; A. Schenk,* Swiss Federal Institute of Technology, Switzerland

The effective conduction band mass m@sub ox@ of a-SiO@sub 2@ has been the subject of extensive studies and considerable controversy, with a defacto value of 0.5m@sub 0@ having been adopted by most researchers.@footnote 1@ The STM based technique of Ballistic Electron Emission Spectroscopy (BEEM) has recently been used to obtain a value of m@sub ox@=(0.63±0.09)m@sub 0@, which was deduced from quantum interference (QI) oscillations in the BEEM current through a 2.8 nm oxide.@footnote 2@ However, the more fundamental issue of the energy dependence of m@sub ox@ has not yet been properly addressed experimentally or theoretically. We report here pronounced QI effects in the BEEM current through 2.2 nm oxides and an assessment of the energy dependence of m@sub ox@(E) obtained from simulations of the transport process. Up to five QI peaks were observed over a kinetic energy range of 2 eV relative to the conduction band minimum (CBM). Peak positions were reproducible to within 0.1 eV for injections at sites previously not exposed to the electron beam. Transmission coefficients (TC) for over-the-barrier injection were calculated by numerically solving the Schrödinger equation, which included both image force effects and an energy dependent m@sub ox@(E). The gradients of m@sub ox@(E) at the energies of the TC maxima were adjusted until a match to the maxima in the data was obtained. With the assumption of a 2.2 nm oxide thickness (measured by ellipsometry, with other measurements in progress), the fits show that m@sub ox@ increases rapidly from 0.60m@sub 0@ near the CBM to 0.86m@sub 0@ 2 eV above the CBM. An expected trend toward m@sub ox@=1m@sub 0@ for larger energies is suggested as well by the results. @FootnoteText@ @footnote 1@A. Schenk and G. Heiser, J. Appl. Phys. 81, 7900 (1997) and references therein. @footnote 2@H.J. Wen, R. Ludeke and A. Schenk, J. Vac. Sci. Technol. B 16, to be published

4:20pm **EM1-ThA8 Ultra Thin Silicon Oxide Film on Si(100) Fabricated by High Purity Ozone at Atmospheric Pressure**, ***K. Nakamura,*** *S. Ichimura, A. Kurokawa,* Electrotechnical Laboratory, Japan*; K. Koike, G. Inoue, T. Fukuda,* Iwatani International Corporation, Japan

Microstructure of electronic devices requires much thinner silicon oxide film so that alternative oxidants must be developed to lower substrate temperature during oxidation. High purity ozone is expected as one of such oxidants because of its higher reactivity not only for adsorption on surfaces@footnote 1,2@ but also for thin film growth@footnote 3@ in comparison with that of molecular oxygen. However, lowering oxidation temperature also needs high dose of ozone to compensate decreasing oxidation rate. We investigated growth kinetics of oxide film under different ozone pressure conditions and succeeded in formation of oxide with the thickness >2nm at room temperature. First we fabricated oxide by exposing Si(100) with the substrate temperatures between 300°C and 700°C to 8x10@super -4@Pa ozone for 90 min. in an UHV chamber. Etching rates by 0.1wt% hydrofluoric acid solution of these SiO@sub 2@ films are equivalent to that of device-grade thermally grown oxide. Etching rate is so sensitive to film density that oxide films made by use of high purity ozone at lower substrate temperatures are expected to be as dense as thermally grown oxide. However, the oxidation rate, especially at oxide thickness >5Å, decreased as oxidation temperature decreased. So we utilized another ozone generator system giving an atmospheric pressure for much higher ozone dose. In this processing, oxide film >2nm was successfully grown on Si(100) even at room temperature. Etching rate of SiO@sub 2@ fabricated on Si(100), for example, at 350°C by this method is almost the same as that of thermally grown oxide or as those with lower ozone dose mentioned above. Effects of such treatment as preoxidation or hydrogen termination on oxidation kinetics and film quality will also be discussed. @FootnoteText@ @footnote 1@ K. Nakamura, A. Kurokawa and S. Ichimura, J. Vac. Sci. Technol. A 15, 2441 (1997). @footnote 2@ K. Nakamura, A. Kurokawa and S. Ichimura, Surf. Interface Anal. 25, 88 (1997). @footnote 3@ A. Kurokawa, S. Ichimura and D. W. Moon, Mat. Res. Soc. Symp. Proc. 477, 359 (1997).

4:40pm **EM1-ThA9 Mixed Silicon Dioxide / Tantalum Oxide Layers for High k MOS Gate Dielectrics Formed by Plasma Oxidation of Si and Ta Using a rf Remote N@sub 2@O Plasma Source**, ***J.J. Chambers,*** North Carolina State University, U. S. A.*; G. Lucovsky, G.N. Parsons,* North Carolina State University

High dielectric constant gate insulators will be needed to minimize gate tunneling in sub-100 nm integrated circuit devices. High k will allow the gate capacitance to scale with gate length without a significant reduction in gate dielectric thickness. Mixing SiO@sub 2@ with high k metal oxides (including Ti or Ta oxides) is expected to increase the dielectric constant without losing the beneficial properties of the Si/SiO@sub 2@ system. We have developed a rf plasma source capable of concurrent remote plasma CVD and separately controlled d.c. sputtering of metals. The motivation of this work is to establish an in-situ process for controlled silicon/high-k interface formation that will be stable during subsequent high-k dielectric deposition. Using an Ar plasma, Ta was sputtered for 1 to 10 minutes leading to controlled coverage onto a cleaned silicon surface. The Ta target was removed from the plasma zone, and the surface was exposed to a remote N@sub 2@O plasma for 10 minutes. After oxidation, XPS and AES were used to characterize Ta, Si and O bonding on the surface. XPS of the oxidized surface shows Ta 4f peaks at 28.4 and 30.3 eV indicative of Ta-O bonds. Si 2p peaks at 101.1 and 104.7 eV are also observed, indicating Si and Si-O bonding. As the surface coverage of tantalum increases, XPS of the oxidized surface shows the O 1s peak at 533.9 eV developing a shoulder at lower binding energy characteristic of O-Ta bonding. This data indicates, for the studied range of small tantalum surface coverage, that the tantalum is completely oxidized forming tantalum oxide and silicon oxide layers. Ellipsometry results indicate the oxide thickness is less than 20 Å. We will discuss the effect of initial Ta layer thickness on oxide formation, and experiments of co-deposition of metal and SiO@sub 2@ to form thin mixed metal oxide / silicon dioxide high dielectric constant films.

5:00pm **EM1-ThA10 Thermal Stability of a-SiNx:H Films Deposited by Plasma Electron Cyclotron Resonance**, *F.L. Martinez,* ***A. del Prado,*** Universidad Complutense de Madrid, Spain*; D. Bravo, F.J. Lopez,* Universidad Autonoma de Madrid, Spain*; I. Martil, G. Gonzalez-Diaz,* Universidad Complutense de Madrid, Spain

Amorphous hydrogenated silicon nitride is widely used in semiconductor devices. Its higher dielectric constant compared to silicon dioxide results in a larger gate insulator capacitance, which in its turn means a larger transconductance and a smaller threshold voltage shift for a given defect charge concentration. A Rapid Thermal Annealing (RTA) post-treatment can improve significantly the properties of the dielectric and the interface. We have analyzed the influence of RTA on Al/SiN@sub x@:H/Si structures with x=1.55. The silicon nitride is deposited by the Electron Cyclotron Resonance plasma method and the films were annealed at temperatures ranging from 300ºC to 1050ºC. Determination of the dangling bond density in the insulator was done with Electron Paramagnetic Resonance, while the density of interface states was obtained from the high-low frequency capacitance method. Resistivity and breakdown field were deduced from current measurements in accumulation. A pronounced dip in the density of dangling bonds is obtained for moderate annealing temperatures, from 1.85E18 cm@super -3@ for the as-deposited film down to 9.58E16 cm@super -3@ at the point of inversion of the trend between 500 and 600ºC. The density of interface states is also reduced in this range of temperatures from 3.6E11 eV@super -1@cm@super -2@ to 1.2E11 eV@super -1@cm@super -2@. Resistivity and breakdown field are maintained in the range 5E14-5E15 @OMEGA@cm and 6.4-6.6 MV/cm respectively up to a temperature of 600ºC. We attribute the improvement of the film properties and interface characteristics to a thermal relaxation and reconstruction of the silicon nitride lattice and its interface with the silicon substrate. In this range of temperatures we did not observe hydrogen evolution from the SiN@sub x@:H lattice. For temperatures above this threshold the electrical properties suddenly deteriorate and the density of dangling bonds increase. At even higher temperatures (above 800ºC) a release of hydrogen from N-H bonds takes place.

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