Electronic Materials and Processing Division
Room 316 - Session EM-MoM

Processing for Advanced Technology

Moderator: D. Temple, Microelectronics Center of North Carolina

8:20am **EM-MoM1 SCALPEL: Projection Electron Beam Lithography**, ***L.R. Harriott,*** Bell Laboratories, Lucent Technologies **INVITED**

SCALPEL (SCattering with Angular Limitation Projection Electron beam Lithography) combines the high resolution and wide process latitude inherent in electron beam lithography with the throughput of a projection system. This approach has the potential to satisfy the lithographic requirements for many IC generations, down to the minimum feature sizes contemplated in the SIA roadmap. We believe that with solid industry support and resources, SCALPEL can be introduced in the 130 nm generation as a replacement for 193 nm lithography for critical levels with reduced cost. SCALPEL masks are expected to be considerably lower cost than optical masks which will require OPC and phase shift for the 130 nm generation. We see the evolution of lithography technology directly from 193 nm to SCALPEL. Throughput is usually thought of as the determining factor in determining the cost of ownership for a lithographic technology. As the limits of optical lithography are pushed toward and beyond sub-wavelength printing, strategies such as phase shifting and optical proximity effect correction (OPC) are required. These technologies add significantly to the cost of the masks and thus, contribute to the cost of wafer printing. The size of the mask factor depends strongly on the mask usage. The number of wafers printed for each mask varies according to the nature of an individual IC business with averages for ASIC at 1000 wafers or less printed per mask. The averages for logic and DRAM are roughly 2000 and 3000 respectively. The total cost of printing a wafer level can, particularly in cases of low mask usage, then be dominated by mask costs and less effected by throughput than has been the case in the past. For SCALPEL, technologies such as phase-shifting and OPC are not required and the resulting mask costs at a given design rule (such as 130 nm) can be significantly less than the corresponding photomask costs. Thus, even though SCALPEL throughput will be less than that for 193 nm optical lithography, the overall cost per level of lithography will be lower due to significantly lower mask costs. We believe that this factor will be a major driving force in determining the timing of the shift away from optical lithography to SCALPEL. We have recently completed our proof-of-lithography system which implements the step-and-scan writing strategy. Our recent data shows that we can write stripes over a 1 X 1 cm field and stitch them together with a raw accuracy of better than 50 nm three-sigma. These measurements were made using box-in-box type patterns at the joining of adjacent stripes across the field. Other errors such as those of the mask beam-writer have not been accounted for in this preliminary experiment. We expect that with further calibration and removal of mask errors that we can achieve stitching to the 10 nm level or less as we have seen in the static stitching data. In order to bring SCALPEL technology to the nest step in its evolution, we are beginning a three-year development program aimed at the full-field high throughput system. The program will focus on larger format mask technology, a high throughput exposure tool, and resist and process development. In this talk, we will outline the status of SCALPEL technology as well as the plans for its continued development. This work has been supported in part by DARPA and SEMATECH

9:00am **EM-MoM3 Fundamental Issues in Wafer Bonding and SOI**, ***U.M. Goesele,*** Max Planck Institute of Microstructure Physics, Germany **INVITED**

During the last decade, wafer bonding has developed from an approach with a "black magic" image to a versatile technology which is partly already used industrially and which allows to avoid the restrictions usually imposed by epitaxy. The science and technology of wafer bonding has been advanced almost independently in three major areas: i) fabrication of SOI (Silicon-On-Insulator) substrates; ii) silicon based micromechanics (where wafer bonding is known as fusion bonding), and iii) bonding of III-V compounds for light-emitting devices and compliant substrates. Present day research aims at understanding and controlling the processes happening at the bonding interface especially for general material combinations and at developing low temperature bond strenghtening approaches for already processed wafers and/or dissimilar materials with different thermal expansion coefficients. Versatile thinning methods for many different technologically relevant materials such as the smart-cut or related methods are also of special interest. The processes involved in atmospheric, low vacuum, or ultra high vacuum wafer bonding at room temperature will be outlined. Hydrogen implantation-induced delamination and layer transfer (smart-cut and smarter cut procedures) will also be discussed for a number of materials including silicon, germanium, diamond, SiC, GaAs and sapphire.

9:40am **EM-MoM5 The Fundamental Mechanisms of Silicon Wafer Bonding and Layer Exfoliation**, ***M.K. Weldon,*** Bell Laboratories, Lucent Technologies **INVITED**

The fabrication of Silicon-On-Insulator (SOI) materials has progressed to such an extent over the past decade that the material specifications are approaching those of bulk silicon and many viable manufacturable processes are now in operation. Silicon wafer bonding is one such commercially-employed approach to SOI synthesis in which two (oxide-terminated) Si wafers are directly bonded under ambient conditions and then annealed to elevated temperatures (1100 C) to form a permanent chemical bond. In the conventional process, the device wafer is subsequently thinned to the required dimensions by extensive grinding/polishing. The limitations imposed by this latter step have recently been removed with the advent of a remarkable new process wherein H+ is pre-implanted into the device wafer at a critical concentration and depth, prior to bonding. Upon subsequent joining to the companion 'handle' wafer and annealing to ~400 C, complete lift-off (exfoliation) of the overlying Si occurs, so that the final SOI structure can now be formed in one elegant annealing step, with thickness uniformities of ~50 Å over the entire wafer. Research has played an important role in the advancement of this field, despite the inherent difficulties in obtaining spectroscopic information about the physics and chemistry of interfaces that typically lie ~500 microns below the surface. In this talk, I will describe how we have obtained@footnote 1@ unprecedented insight into the thermal evolution of the buried interfaces that comprise both the bonded and the exfoliation interfaces, using a wide variety of different experimental probes in combination. In particular, I will highlight the pivotal role of infrared spectroscopy in delineating the microscopic mechanisms that permit the intimate chemical bonding of two wafers and the transformation of isolated hydrogenated defects into extended internal cracks that ultimately lead to exfoliation of macroscopically large areas of Si. @FootnoteText@ @footnote 1@M.K. Weldon, V.E. Marsico, Y.J. Chabal, A. Agarwal, D.J. Eaglesham, J. Sapjeta, W.L. Brown, D.C. Jacobson, Y. Caudano, S.B. Christman and E.E. Chaban, J. Vac. Sci. Technol. B 15, 1065 (1997).

10:20am **EM-MoM7 DARPA High Definition Systems Program**, ***B.E. Gnade,*** Defense Advanced Research Projects Agency **INVITED**

The DARPA High Definition Systems (HDS) Program has the overall goal to meet the diverse, but specific, needs for information display for the Department of Defense. The goals of the HDS program include increasing power efficiency, reducing weight, and improving the overall ruggedness of display systems. The HDS program is also actively working to transition DARPA-funded display technologies into specific military applications. A brief review will be presented which shows how new display technologies are being used in the military, as well as examples of new technologies which are being supported under the DARPA HDS program.

11:00am **EM-MoM9 Field Emission Energy Distributions from Silicon Field Emitter Arrays**, ***J.L. Shaw,*** *H.F. Gray, K. Hobart,* Naval Research Laboratory

A great deal of work on field emitter array (FEA) surface coatings, treatments, and "conditioning" effects has been has been reported in hopes of improving the maximum current, robustness, and transconductance. However, the typical current-voltage diagnostic technique has limited utility in understanding the effects of such treatments. Field enhancement and work function effects are difficult to separate using I-V measurements and assuming the classical Fowler-Nordheim theory. Furthermore, the I-V characteristics typically vary with time and emission even in UHV. To better understand the emission process, we have measured FEA emission energy spectra. Our equipment includes a hemispherical analyzer and allows in-situ wafer probing and simultaneous I-V characterization. The spectra we obtain include structure at lower energies than reported from single, macroscopic, clean silicon tips. Since the emission energy relative to the bulk Fermi level represents a loss, such spectra are of considerable interest. The spectra change as a function of emission current, conditioning, and processing. In some cases we find energy losses in excess of 10 volts. Such losses may explain why failures can occur at emission levels below 1uA, even though calculations (that assume straightforward Joule and Nottingham heating) predict no temperature increase at emission currents below 100uA. Our measurements suggest that both the emission current and dissipated energy can be strongly influenced by the presence of surface states. Thus detecting such effects is

likely to prove useful in improving FEA emission uniformity and total current density.

11:20am **EM-MoM10 Effects of Oxygen on Silicon and Platinum-coated Silicon Field Emitter Arrays**, ***W.D. Palmer***, *D. Temple, D.G. Vellenga, L.N. Yadon, G.E. McGuire,* Microelectronics Center of North Carolina

Field emission depends strongly on the work function of the emitter surface. At any vacuum level, molecules will adsorb on the emitter surface and change the work function by forming a chemical bond with the emitter material. . This study addresses this problem and one possible solution by testing silicon and platinum-coated silicon field emitter arrays in oxygen over a wide pressure range similar to that expected in commercial field emission flat panel displays. Platinum is less likely than silicon to form these bonds, and so should exhibit less sensitivity to the ambient gases in the display panels. The experiments were undertaken using silicon and platinum-coated silicon gated field emitter arrays fabricated at MCNC. The arrays were initially operated at base pressure (5x10@super -9@ Torr) using an automated system to guarantee that all tests were performed consistently. After collecting current versus voltage (I-V) curves for each device at base pressure, a leak valve was used to introduce oxygen at the target pressure. The arrays were then operated with a constant voltage on the gate electrode until the emission current stabilized. In this study, the data is shown as a function of exposure, the product of pressure and time, to normalize the results. I-V curves were collected at the target pressure after stabilization, then the leak valve was closed and the chamber was pumped back to base pressure. Finally, I-V curves were again collected at base pressure to verify that the array had recovered to its initial level of performance. The data collected on silicon and platinum-coated silicon field emitter arrays will be shown and compared. This work was performed under the DARPA/ETO High Definition Systems program, contract number N00014-96-C-0283.

11:40am **EM-MoM11 Improved Performance in Thin Film Electroluminescent Phosphors by Fluxing**, ***J.S. Lewis***, *K.E. Waldrip, M.R. Davidson, D. Moorehead,* University of Florida, Gainesville, U.S.*; S.S. Sun,* Planar Systems, Inc.*; P.H. Holloway,* University of Florida, Gainesville

The brightness and efficiency of AC thin film electroluminescent devices (ACTFELD's) which use ZnS:Mn as the thin film phosphor have been improved by the incorporation of various fluxes. The brightness of fluxed, sputter deposited films were doubled and the efficiencies are nearly tripled compared to unfluxed, sputter-deposited films. In addition, the improved brightness and efficiency values surpass those achieved by the standard evaporated or ALE (atomic-layer epitaxy) grown devices. The fluxes have been incorporated both during and after sputter deposition of the phosphor, and a post-deposition anneal is required. Data will be presented which demonstrate improved brightness and efficiency. The flux treatment gave significant improvement in the degradation of luminescence after accelerated device operation. Microstructural changes that result from fluxing as detected by X-ray diffraction, transmission electron microscopy, and scanning electron microscopy will be presented.

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