Electronic Materials and Processing Division
Room 316 - Session EM-MoA

Future Issues in Electronics and Photonics

Moderator: H.A. Atwater, Caltech

2:00pm **EM-MoA1 Pathways Toward Chemically Assembled Electronic Nanocomputers*, J.R. Heath,*** University of California, Los Angeles*; R.S. Williams, P.J. Kuekes,* Hewlett Packard Corporation **INVITED**

Many ideas for alternatives to CMOS-based VLSI manufacturing have been proposed as new paradigms for computer fabrication. These ideas include quantum computing, molecular computing, and chemically-assembled electronic nanocomputers. Of these three, only electronic nanocomputers can potentially build upon the foundation of CMOS architectures, and, as such, they hold the potential for relatively near-term realization. However, even the simplest of computational tasks have yet to be demonstrated for electronic nanocomputers. From a chemist's point of view, there are two major differences between anything fabricated chemically, and a current microchip. The current microchip is complex and is the result of manufacturing perfection, while anything that is chemically synthesized is likely to be ordered (crystalline) and imperfect. Thus, in many ways, the chemist's task is to design a system from which perfect complexity can be extracted from imperfect order. In this presentation, I will discuss an ongoing HP/UCLA project in which we are attempting to build an electronic nanocomputer. Architectural considerations will be stressed, and experimental progress towards building the nanocomputer will be discussed.

2:40pm **EM-MoA3 Room Temperature Silicon Single Electron Memory and Switch and Nanoimprint Lithography*, S.Y. Chou,*** Princeton University **INVITED**

The paper presents two recent progresses in developing single electron devices that can operate at room temperature and one breakthrough in nanopatterning. The first is a single-electron MOS memory in crystalline silicon, that has a channel width (~10 nm) and a nanoscale polysilicon dot (~7 nm by 7 nm) as the floating gate embedded between the channel and a control gate.@footnote 1@ It is observed that storing one electron on the floating gate can significantly screen the channel from the potential on the control gate, leading to a threshold voltage shift. The second progress is a silicon single electron switch, that has a small silicon dot (~12 nm in diameter) inside the channel and separated from the source and drain by two thin tunneling barriers.@footnote 2@ As a gate modulates the electron population inside the dot, the drain current oscillates at room temperature. Each oscillation is attributed to electron tunneling through a discrete single electron level inside the dot. Finally, nanoimprint lithography is a new lithographic mehtod that has achieved sub-10 nm feature size with high throughput and low cost, paving the road for manufacturing silicon single electron devices.@footnote 3@ @FootnoteText@ @footnote 1@L. Guo, E. Leobandung and S.Y. Chou, Science, vol. 275, 649-651, 31 January, 1997. @footnote 2@L. Zhuang, L. Guo, and S.Y. Chou, IEDM, Dec. 8-10, 1997. @footnote 3@S.Y. Chou, P.R. Krauss, W. Zhang, L. Guo and L. Zhuang, J. Vac. Sci. Technol. B 15(6), 2897 (1997).

3:20pm **EM-MoA5 Terabit Integration: New Ideas, Need for New Materials*, K.K. Likharev,*** State University of New York, Stony Brook**INVITED**

The electronics industry predicts that the current progress in scaling down silicon MOSFETs will lead eventually to dynamic random-access memories with a density of the order of 5 Gbits/cm@super 2@ and integration scale up to 64 Gbits. Further progress in this direction is, however, in doubt, mostly because of problems with the storage capacitance scaling. The situation may be changed by the recently proposed@footnote 1@ "crested" tunnel barriers, with an electrostatic potential maximum in the middle. In these barriers, applied voltage increases the barrier transparency much more quickly. Calculations have shown that crested barriers may combine long retention time (say, 10 years) with fast write/erase time (below 10 nanoseconds). This radical improvement may be used, first of all, in nonvolatile random-access memories ("NOVORAM"). Using dual-gate, nanoscale MOSFETs with ballistic electron transfer along undoped channels,@footnote 2@ NOVORAM cells are scaleable to a minimum feature size about 6 nm, corresponding to a memory density of 100 Gbits/cm@super 2@, and apparently integration scale up to 16 Tbits. Beyond this frontier, NOVORAM may be challenged by SET/FET hybrid memories@footnote 3@ with dynamic read-out using single-electron transistors (SETs) in background-charge-insensitive mode. Analysis shows that these memories may be scaled to the 2 nm minimum feature size, enabling integration up to 64 Tbits. Moreover, there is an opportunity to combine crested barriers and SET/FET hybrids in a system for electrostatic data storage with density beyond 100 Gbits per square inch. In my presentation at the meeting, I will describe these encouraging prospects in detail, and also discuss the requirements to materials for their practical implementation. @FootnoteText@ @footnote 1@K.K. Likharev, in: GOMAC'98 Technical Paper Digest, p. 35. @footnote 2@F. Pikus and K. Likharev, Appl. Phys. Lett. 71, 3661 (1997). @footnote 3@K.K. Likharev and A.N. Korotkov, in: Proc. of 1995 ISDRS, p. 355

4:40pm **EM-MoA9 Oxide-Confined Vertical Cavity Surface Emitting Lasers using Quantum Well and Quantum Dot Active Regions*, D. Huffaker,*** University of Texas, Austin **INVITED**

There is increasing interest in low power optoelectronics including ultralow threshold semiconductor lasers for use in optical interconnect applications. The oxide-confined vertical cavity surface emitting laser (VCSEL) is a potential candidate for such applications because of the promising device results which have been demonstrated to date. At the University of Texas we have focused on minimizing optical loss from the lasing mode by lateral index confinement and high contrast mirrors. This talk will overview our device structures, the selective oxidation processing and low threshold quantum well VCSEL results. The low loss VCSL cavity may be especially important in realizing 1.3µm VCSELs grown on a GaAs substrate using an InAs/GaAs QD active region as the QDs have limited gain at this long wavelength. To date, we have achieved a 1.15µm GaAs-based VCSEL using the InAs/GaAs QDs. We will also discuss very recent data characterizing ultranarrow electroluminescence spectra from a large ensemble of quantum dots at very low current densities.

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