Electronic Materials and Processing Division
Room 314/315 - Session EM+PS-ThM

Processing of High K Dielectrics for DRAMs

Moderator: K.R. Milkove, IBM T.J. Watson Research Center

8:20am **EM+PS-ThM1 Growth and Characterization of Ba@sub 0.6@Sr@sub 0.4@TiO@sub 3@ Thin Films on Si with Pt Electrodes**, ***L. Kinder***, *I.L. Grigorov, C. Kwon, Q.X. Jia,* Los Alamos National Laboratory*; L. Luo, J. Zhao,* Applied Materials, Inc.

The application of high dielectric constant materials like barium strontium titanate in dynamic random access memories requires the integration of these materials into the existing Si technology. In this study, pulsed laser deposition was used to grow Ba@sub 0.6@Sr@sub 0.4@TiO@sub 3@ (BST) thin films on Si with Pt electrodes. Through scanning electron microscopy, x-ray diffraction, and electrical characterization, the Pt/BST/Pt capacitor processing on Si has been optimized. BST films on Pt sputtered at high power tends to show high leakage current. However, high leakage current is prevented if the Pt is sputtered at low powers. Low power deposition leads to not only smooth Pt film but also less hillocks. The smoother Pt electrodes allow the BST to grow with greater crystallinity. 150 nm BST on Pt shows a dielectric constant over 400 and dielectric loss of 0.01 at 10 kHz. The quality of the dielectric can be further improved by first depositing a thin seed layer of BST at lower temperatures. We have successfully used 20 nm BST deposited by metal-organic chemical vapor deposition as a seed layer to improve the over all device performance. The influence of interface and of initial nucleation of BST films on the structural and dielectric properties of the thin film capacitors will be also discussed.

8:40am **EM+PS-ThM2 Synthesized Single Crystalline Ba@sub (1-x)@Sr@sub x@TiO @sub 3@ Thin Films for DRAM Application**, ***F.F. Feng***, University of Houston*; C.L. Chen, Z.H. Zhang,* University of Houston, U. S. A.*; Y. Liou, P. Jin,* University of Houston*; W.K. Chu,* University of Houston, U. S. A.*; C.W. Chu,* University of Houston

Perovskite Ba@sub (1-x)@Sr@sub x@TiO@sub 3@ thin films have been synthesized on (001) LaAlO@sub 3@ and (001) SrTiO@sub 3@ substrates with SrRuO@sub 3@ or Pt bottom electrodes by pulsed laser ablation. Extensive X-ray diffraction, rocking curve, and pole-figure studies suggest that the as-grown films are (00l) oriented with single crystalline quality. RBS studies indicate that the epitaxial films have excellent crystalline quality with an ion beam minimum yield of only 2.6 % or less, suggesting that the crystallinity of the as-grown films can be compared with the single crystal silicon. Atomic force microscopy studies indicate that the as-epitaxial films are atomic smooth under the selected growth conditions. The dielectric property measurements show room temperature values of the relative dielectric constant and loss tangent of larger than 750 and 0.005, respectively.

9:00am **EM+PS-ThM3 Scanning Capacitance Imaging for Evaluation of High-k Dielectric Oxide Materials**, *Y. Yamaguchi, K.P. Wiederhold, B.D. White, N.E. Wittry,* ***H.C. Galloway***, Southwest Texas State University

We have used scanning capacitance imaging to measure the dielectric properties of oxide materials such as BST which have large dielectric constants (high-k). These materials are of interest as potential replacements for the dielectric in memory devices due to their increased capacitance per unit area. Several scanning capacitance methods have been developed using modified atomic force microscopes and they are actively used to measure quantities such as the thickness of SiO@sub 2@ layers or the doping levels across a p-n junction. We will discuss how this technique can be used as a diagnostic tool when applied to the high-k oxides. First, the measurement of the dielectric properties on a local scale may help to identify the causes of failure modes in materials. As an example, we will report on local variations of the dielectric constant observed in films of BST grown by RF planar magnetron sputtering. Second, we have used scanning capacitance to evaluate films of novel oxide materials grown by Dual Ion Beam Sputtering.@footnote 1@ The advantage of Scanning Capacitance Microscopy is that the relative merits of different growth conditions can be rapidly assessed and compared to each other or to a reference standard. This allows us to investigate new materials or deposition conditions without having to form complete devices for analysis. By identifying the most promising growth conditions that yield high dielectric constants, uniform films, and low leakage currents we can speed up the process of testing new growth methods and materials.

@FootnoteText@ @footnote 1@P. Perera, R. Selestino, and C.J. Gutierrez, Department of Physics, Southwest Texas State University

9:20am **EM+PS-ThM4 Characterization of Thermal Annealing of Tantalum Pentoxide for High-k Dielectric Applications**, ***R.L. Opila***, *J.P. Chang, G.B. Alers,* Bell Laboratories, Lucent Technologies

Tantalum pentoxide is being studied as an alternative high dielectric constant material for storage capacitors or gate dielectrics. Since the oxide layers are thin, even for high dielectric constant materials, interfaces between the tantalum pentoxide and other thin film materials can greatly affect device electrical properties. This paper focuses on analyzing the bulk properties of the Ta@sub 2@O@sub 5@ film and the Ta@sub 2@O@sub 5@/TiN interface to assess a new TiN/Ta@sub 2@O@sub 5@/TiN storage capacitor structure that has lower contact resistance and higher specific capacitance than conventional poly-Si based capacitors. The effect of thermal annealing on the electrical performance of the capacitor will be presented. Angular Resolved X-ray Photoelectron Spectroscopy (ARXPS) has been used to characterize the interfacial composition and stoichiometry of tantalum pentoxide deposited by CVD processes at low temperatures. The amount of carbon incorporated in the film during the CVD process decreases with increasing process temperature. Reduced leakage current has been observed as the concentration of carbon in the film increases. Formation of TiO@sub 2@ was observed at the Ta@sub 2@O@sub 5@/TiN interface at an RTA temperature of 450°C. Significant amounts of titanium suboxides are also observed at the Ta@sub 2@O@sub 5@/TiN interface. The imperfect interface is thought to reduce the specific capacitance and increase leakage currents, perhaps through partial reduction of the Ta@sub 2@O@sub 5@. Correlation between the interface chemical states and the electrical performance will be presented.

9:40am **EM+PS-ThM5 Structural Properties of Ultrathin Films of High Dielectric Constant Materials on Silicon**, *E. Gusev,* IBM T.J. Watson Research Center*; H.C. Lu, T. Gustafsson,* ***E. Garfunkel***, Rutgers University*; G.B. Alers,* Bell Laboratories, Lucent Technologies

The high tunneling rates in ultrathin gate oxides is driving the search for higher-K replacement dielectrics in silicon microelectronics. Ta@sub 2@O@sub 5@ and several other metal oxides are now attracting the attention of the device community. One problem that plagues the use of metal oxides on Si is the formation of an interfacial SiO@sub 2@ layer; such layers limit the capacitance and can degrade the electrical properties of the gate structures. We have examined the composition of interfacial layers of several high dielectric constant oxide systems using high resolution medium ion energy scattering. We find that the interfacial region is best described as neither Si/SiO@sub 2@/metal-oxide nor Si/metal-oxide, but can be viewed as a compositionally graded oxide with a dielectric constant significantly higher than that of pure SiO@sub 2@ (as inferred from electrical measurements). Annealing changes the near-interfacial composition substantially. When post anneal temperatures are kept low, stable composite oxide structures (with physical thickness greater than 7nm) can be obtained that demonstrate good electrical properties and an effective SiO@sub 2@ thickness of less than 2 nm.

10:00am **EM+PS-ThM6 Etching of High Dielectric Constant Materials for DRAMs and Ferroelectric Materials for FeRAMs**, ***L.G. Jerde***, *A. Cofer, K. Olson, P. Rajora, S.P. DeOrnellas,* Tegal Corporation **INVITED**

The introduction of ferroelectric and high dielectric constant films and their associated metals, barrier materials and adhesion layers for DRAM, embedded DRAM and FeRAM applications are driving some of the most challenging etch requirements in the IC fabrication industry. The specifications resulting from these requirements range from very aggressive profile and critical dimension control, to etch selectivities, contamination and damage, defects and chamber cleaning frequency. Some of the most difficult of these requirements are a result of the design rules that will be used in production for the DRAM applications (i.e., 0.15 m and below). The inherent involatility of the etch products of these materials is another key factor contributing to the difficulty in meeting the requirements. In this paper we will present and discuss the etch requirements for these materials, the reactor technology we use to etch them, selected process and manufacturability results for these materials and future directions for this work.

10:40am **EM+PS-ThM8 Patterning of Reactively Sputtered Tantalum Pentoxide, a High Epsilon Material, by Plasma Etching**, *L.B. Jonsson, F. Engelmark, J. Du, C. Hedlund,* Uppsala University, Sweden*; U. Smith,* Ericsson Components AB, Sweden*;* ***H.-O. Blom****,* Uppsala University, Sweden

The large size of integrated capacitors is a problem today. The capacitors can easily cover a major part of the total chip area. By using a high epsilon material as the dielectric material in the capacitor the size can be reduced significantly. One very promising candidate is Tantalum pentoxide (Ta@sub2@O@sub5@) which has an epsilon of 25 compared to Silicon dioxide which has 3.9. In order to make integrated capacitors the Tantalum pentoxide must be patterned. We have investigated and optimized dry etching processes for realizing a complete capacitor structure. One process for etching the Tantalum pentoxide on a back contact made of poly-silicon and one process for etching contact holes, in silicon dioxide, down to the Tantalum pentoxide. Data from Reactive Ion Etching (RIE) as well as for Inductively Coupled Plasma (ICP) processes will be presented.

11:00am **EM+PS-ThM9 The High Temperature Platinum Etching Using Titanium Layer***, **H.-W. Kim**, B. Ju, B. Nam, W. Yoo, C.J. Kang, T.-H. Ahn, J. Moon, M.Y. Lee,* Samsung Electronics, Co., Korea

1. Introduction: It is necessary to use the platinum as a bottom electrode material of the BST capacitor in highly integrated deveces, however, the Pt etching of the fine patterns is difficult due to the inherent non-reactivity of platinum. It is revealed that the Pt etch slope of 80° was attained by O@sub 2@/Cl@sub 2@ chemistry by elevating the substrate temperature up to 160°C. This result is thought to be due to the reaction of O species with Ti layer and analyzed by TEM, XPS and AES. 2. Experimental & Results: As an experimental setup for high temperature etching, the modified chiller using Galden HS260 (B.P.=270°C) was chosen. The oxide 5000Å/ Ti600Å/ Pt 2000Å structure was used and the O@sub 2@/Cl@sub 2@ (O@sub 2@ = 80%) gas was chosen as an etchant combination in MERIE system. The change of the Pt etching profile at 100°C, 130°C, 160°C, respectively was investigated.The Pt etch slope does not depend on the substrate temperature up to the just etch time, the etch slope of the 160°C-sample was about 80° after 100% overetch and the Ti mask was not eroded significantly. It appeared that the titanium mask of 100°C, 130°C samples were eroded considerably, The Pt etching results of 160°C with Ti, TiN and TiO@sub 2@ layer were compared (not shown). TiN and TiO@sub 2@ layer does not help attaining high Pt etch slope even with the thermal heating. From the above result, it is surmised that the change or stabilization of Ti layer through the reaction/diffusion of O atoms during plasma etching plays a major role in attaining the higher Pt etching slope. From the XTEM investigation of the 160°C-etched one, the center of the Ti layer stays crystalline, however, the edge of the Ti layer became amorphous and the oxygen content increased up to more than 50%, by EDX analysis. The XPS analysis of 100-Ti layer showed that the considerable amount of Ti-Ti bond changed to the Ti-O bond during the O@sub 2@/Cl@sub 2@ plasma treatment. The AES analysis confirmed the above phenomena. 3. Conclusions: The etching slope of Pt was improved by the reaction of the mask material with the etching species, not by the reaction of Pt itself. The optimal overetching helps to attain the higher etch slope as long as the Ti mask stays. High temperature processing helped the duration of the titanium mask by activating the reaction of Ti with O-species.

11:20am **EM+PS-ThM10 Removal of Sidewall Re-depositions Formed by Reactive Ion Etching of Platinum for Embedded DRAM Applications**, *H.M. Ranpura, D.H. Butler,* ***S.P. Beaudoin****,* Arizona State University*; C.J. Tracy, L. Chang,* Motorola Semiconductor Products Sector

Removal of platinum sidewall re-depositions (SRDs) formed due to patterning of electrodes due to reactive ion etching (RIE) for an embedded dynamic random access memory (DRAM) project has been investigated. A serious problem in integrating these devices is the re-deposition of non-volatile etch products onto the pattern sidewall. Removal of these SRDs without damaging other exposed materials is a challenging process. A mixture of argon (Ar) and chlorine (Cl@sub 2@) plasma was used to etch the platinum electrodes. Following the etching step the wafers were processed in an oxygen plasma to remove the photoresist on the wafer. Results are presented for post-ashed wafers that were heated at different temperatures for varying times in different ambients. Following heating wafers were cleaned in aqueous hydrochloric acid (HCl). Results are also presented for ultrasonic cleaning of wafers in HCl.

11:40am **EM+PS-ThM11 Study on Surface Reaction of (Ba,Sr)TiO@sub 3@ Thin Films by High Density Plasma Etching***, **S.B. Kim**, C.I. Kim, E.G. Chang,* Chung-ang University, Korea

Ferroelectric devices are attractive for dynamic random access memories (DRAMs) applications because of high dielectric constant. Using ferroelectric device structure, manufacturing cell capacitance of highly integrated memory device is possible. Small feature size requires anisotropic etching. Since research of (Ba,Sr)TiO@sub 3@ thin films etching is not widely, we studied on surface reaction of (Ba,Sr)TiO@sub 3@ thin films by high density plasma etching. (Ba,Sr)TiO@sub 3@ thin films were etched with an Inductively coupled plasma (ICP) by varying the etching parameter such as BCl@sub 3@/C@sub 2@F@sub 6@/Ar gas mixing ratio, RF power, and pressure. Etching effect were investigated in terms of etch rate, selectivity. In this study, (Ba,Sr)TiO@sub 3@ etching mechanism was investigated with XPS (X-ray photoelectron spectroscopy) and OES (Optical emission spectrometry) and QMS (Quadrupole mass spectrometry). Ion current density was measured by using single Langmuir probe. Surface of etched (Ba,Sr)TiO@sub 3@ investigated with SEM (Scanning electron microscopy).

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