Plasma Science and Technology Division
Room: 23 - Session PS-TuM

Advanced FEOL/Gate Etching
Moderators: Kazunori Koga, Kyushu University, Japan, Erwine Pargon, CNRS-LTM, Université Grenoble Alpes, France

8:00am **PS-TuM1 Highly Selective Silicon Dry Chemical Etch Technique for 7nm FinFET Technology and Beyond**, *Z. Bi, **Thamarai Devarajan**, L. Young, B. Miao, S. Devries, N. Loubet, C. Yeung, J. Zhang, A. Greene, H. Zhou, M. Wang, J. Strane,* IBM Semiconductor Technology Research, *Y. Yao,* IBM, *D. Canaperi, C. Surisetty*, IBM Semiconductor Technology Research

With transistor scaling in 7nm technology and beyond, fin spike removal and dummy gate silicon pull are considered to be among the most challenging hurdles in FinFET process development. In this paper, we present a plasma free dry chemical etch technique utilizing NF_3 and H_2 for selective etching of single crystal and polycrystalline silicon at various FinFET device process steps. It was demonstrated that this technique could completely remove poly silicon in vertically high aspect ratio (AR>5) nanosheet FinFET gates with larger process window (overetch budget ~200%), lower gate leakage current and much higher device yield, compared to the technique used in previous generations. Proper surface preparation, queue time control, and etch byproduct removal strategies are discussed. The residue-free etch and etch by-product sublimation mechanisms are also investigated by High Resolution Electron Microscopy (HREM) and Fourier Transform Infrared Spectroscopy (FTIR) surface analysis.

8:20am **PS-TuM2 Anisotropic and Selective Isotropic Etching of Si / SiGe Multilayers in Surface Wave Plasmas**, ***Nick Joy**, S.A. Voronin, P. Biolsi,* TEL Technology Center, America, LLC, *A. Ranjan*, Tokyo Electron Miyagi Limited, Japan

As the feature size of planar devices reaches some fundamental limitations, the continuing drive to increase device density has led to new 3D designs such as fin FETs, nanowire, and vertical FET designs. These innovations bring their own set of challenges for etch applications. While planar devices relied more on anisotropic etching, 3D devices require more isotropic etch capabilities with high selectivity between different materials. For example, one strategy to form nanowire channels is to use multilayered Si/SiGe films that are etched vertically with an anisotropic method to define the width of the wire, and then etched laterally with a selective process that leaves isolated nanowires and allows for deposition of wrap-around gates. Such processes may require either Si selective or SiGe selective isotropic etch capabilities. These abilities have been demonstrated with a RLSA™ plasma etch chamber. Having spatially separated plasma generation and plasma processing regions, RLSA™ etchers benefit from a very low electron temperature (Te~1eV) and low self-bias voltage (i.e. low ion energy) radical-rich discharge. These conditions allow both isotropic and anisotropic selective etching of different materials.

Whether the process is selective to SiGe or Si depends on the chemistry. Generally, it is easier to etch SiGe selective to Si using fluorocarbon plasmas. The dependency of SiGe recess profiles on pressure, power, and non-fluorinated gas addition show trends that are essentially non-selective to highly SiGe (30% Ge) selective using CF4 based processes. Si selective processes are more difficult to achieve and are sensitive to specific process parameters. However, it is possible to reverse selectivity from Si:SiGe < 1 to Si:SiGe > 1 using SF6 based processes. While the etch mechanism is due to fluorine radicals in both cases, Si:SiGe < 1 may be the result of either lower bond energy of Si-Ge compared to Si-Si, or band gap narrowing with Ge addition[1]. For Si:SiGe > 1, the etch rate of SiGe is inhibited with SF6 gas under the right process conditions, which may be due to preferential deposition of an involatile sulfur blocking layer [2]. This work demonstrates the range of selectivity and isotropic etch capabilities between Si and SiGe using RLSA™.

[1] S. Borel, V. Caubet, J. Bildea, A. Cherif, C. Arvet, C. Vizioz, J.M.Hartmann, G.

Rabillé and T. Billona. ECS Transactions, 3 (7) 627-642 (2006)

[2] G. S. Oehrlein, T. D. Bestwick, P. L. Jones, M. A. Jaso, and J. L. Lindstrorn. J. Electrochem. Soc. 138, 1443 (1991).

8:40am **PS-TuM3 Control of Anisotropic Simultaneous SiGe-Si Etching for Dual Channel Fin Applications**, ***Yohei Ishii**, M. Walker, R. Scott-McCabe, A. Yu,* Hitachi High Technologies America, Inc., *K. Okuma,* Hitachi High-Technologies Corp., Japan, *K. Maeda, J. Sebastian, J. Manos*, Hitachi High Technologies America, Inc.

As a result of miniaturization by the semiconductor industry to follow the pace of Moore's law, new design approaches to manufacturing have been introduced. Logic device structures have transitioned from traditional planar designs to three dimensional Fin-type Field Effect Transistors (FinFET). This structure change has achieved improved device characteristics such as higher drive currents and lower transistor leakage. To further enhance FinFET electrical performance, a potential approach is the use of high mobility channel materials such as silicon germanium.

In current fabrication schemes, achieving vertical fin profiles and controlling RIE lag are typical issues associated with the fin etch process. However, with the use of silicon in n-FETs and silicon germanium in p-FETs, new etching challenges such as material-dependent etching rate differences have emerged. During the fin etching process, the silicon and silicon germanium must now be etched simultaneously. Silicon germanium etching characteristics have been studied and the results indicate that, with conventional halogen chemistries, the etch rate of silicon germanium is greater than silicon [1]. Should future technology nodes adopt silicon-germanium as a high mobility channel material, etching processes must consider how to control these material-dependent phenomena.

In this presentation, we will introduce an etching process which can be used for dual channel SiGe/Si fin etching. The result shows that the etched amount difference between silicon germanium and silicon can be controlled from a positive value (silicon germanium etching rate is greater than silicon etching rate) to a negative value. Surface analyses were also utilized to further understand the process and the mechanism. Details will be discussed in this presentation.

[1] G.S. Oehrlein, Y. Zhang, G. M. W. Kroesen, E. de Fresart, and T. D. Bestwick, Appl. Phys. Lett. **58**, 2252 (1991)

9:00am **PS-TuM4 Etch Rate and Profile Tailoring of Si and SiO_2 through Laser-Stimulated Thermal Desorption**, ***Jason Peck**, D.N. Ruzic*, University of Illinois at Urbana-Champaign

In this work, laser exposure was coupled with plasma etch processes for local etch rate enhancement (and under some conditions, etch activation). Materials were tested which are most-frequently used in semiconductor devices – namely Si, SiO_2, and Cu. A 100 Hz, 7 ns pulse width Q-switched Nd:YAG laser was applied at its 1064, 532, and 266 nm modes. Using the 532 nm line on Si (40 mJ/cm^2/pulse) with a radiofrequency inductively-coupled plasma (RF-ICP) source placed upstream, laser etch enhancement effect was 4 Å /s in 50:4 sccm Ar/SF_6, and 3 Å /s etch enhancement at 50:8:2 sccm $Ar/C_4F_8/O_2$. With no O_2 flow in a 50:8 sccm Ar/C_4F_8 chemistry in an RF capacitively-coupled plasma (RF-CCP) source with a measured self-bias of -140 V, etch activation was seen at 0.62 ± 0.07 W/cm^2 (6.2 ± 0.7 mJ/cm^2), with etch rates linearly increasing with laser intensity. The 266 nm line saw etch activation at roughly the same intensity, though etch rate scaling with laser intensity was roughly 6 times higher than 532 nm, corresponding to the drastically-larger absorption depth of 266 nm in Si. No etch enhancement was produced in either chemistry for SiO_2 due to its transparency across the UV-VIS-NIR spectrum, even at 266 nm. CF_x polymer thinning was observed on both Si and SiO_2 at 266 nm but only on Si at 532 nm, indicating a thermally-driven desorption mechanism which relies on heating the material beneath.

It was shown that continuous wave (CW) laser sources of 405, 455, and 520 nm were unable to produce etch enhancement even up to intensities of 200 W/cm^2, demonstrating the necessity of rapid heating of the Q-switched Nd:YAG source (~10s of MW/cm^2 over 7 ns) to temporarily but drastically increase wafer surface temperature. COMSOL simulations showed that a Si surface over the duration of a 532 nm laser pulse would increase temperature by 2.7° C per mJ/cm^2 – a reliably linear rate, even at high intensity. Testing of highly-doped Si wafers revealed a substantial increase in etch enhancement – 10^{19} and 10^{21} cm^{-3} P-doped wafers showed 1.7× and 3.7× higher etch rates over intrinsic Si, respectively. The increased absorption coefficient in these doped wafers confirmed that the etch enhancement mechanism was due to desorption of etch products through thermal heating, rather than through photolytic bond breaking.

Finally, etch tests of 100 nm full-pitch, 100 nm deep trenches showed the ability to tailor etch profile based on wafer orientation. Polarization parallel to the trench line enhanced etching at the top of the features, while perpendicular to the trench line increased trench bottom etch rate.

9:20am **PS-TuM5 Prediction and Control of Fluctuation of Etching Properties by Simulation Technology**, ***Nobuyuki Kuboi***, *M. Fukasawa, T. Tatsumi*, Sony Semiconductor Solutions Corporation, Japan **INVITED**

Fluctuations of etching properties such as the etched profile and damage distribution can affect the performance of advanced CMOS devices, making the prediction and control of these properties vital for mass production. However, the fluctuations mechanisms are not perfectly understood because of equipment limitations in the plasma monitoring systems used in mass production. Therefore, as a predictive technology, a plasma etching simulation was developed that considers the physical and chemical aspects of the plasma and the etched surface.

We modeled CH_xF_y plasma for SiN etching with a CCP system, taking into account the interaction between the bulk region and the chamber wall surface, and simulated the hydrogen (H) density distribution and H Balmer line emission (virtual OES) [1][2]. From comparisons with experimental OES, the reaction probabilities of H with varying chamber wall conditions (Si, SiO_2, polymer) were derived as 0.5, 0.06, and 0.1, respectively. Using these values, the incident H radical flux was calculated, and found to correlate with the SiN etch rate. This signifies that flux fluctuation is important for controlling the SiN etch rate.

To predict the etched profile and damage distribution for SiN, SiO_2, and Si etching, we developed a new simulation technique using an extended 3D voxel model. This included a Slab model [3] that divides the surface region into several thin slabs and time-dependently solved the surface reactions of its reactive and deposition layers, as well as the depth. We demonstrated SiN sidewall (SW) etching for MOSFET and bulk FinFET with CH_xF_y plasma, successfully describing the etching properties. In addition, a local damage distribution can be seen around the SW edge and in the Si fin, which is difficult to find by experimental analysis. Furthermore, our simulation found that a large amount of Si damage in the Si substrate is caused during SiO_2/Si contact hole etching despite the high SiO_2/Si selectivity (>20) [4], which also exhibits time-dependence. Also, fluctuations of the CD and the Si recess during Si gate etching by HBr/O_2 plasma are greatly affected by the byproduct ($SiBr_x$), exhibiting a dependence on the factor $(R_G+R_S)S$ that includes the wafer (R_G) and chip (R_S) open area ratios, and pattern solid angle (S) [5].

These simulation technologies give us useful knowledge for optimizing the chamber wall condition, plasma etching process, and pattern design for advanced CMOS devices.

[1] Kuboi *et al*., JJAP **49**, (2010) 08JD01.

[2] Fukasawa *et al*., JJAP **48**, (2009) 08HC01.

[3] Kuboi *et al*., JVST A **33**, (2015) 061308.

[4] Nakamura *et al*., JVST A **25**, (2007) 1062.

[5] Kuboi *et al*., JVST A **31**, (2013) 061304.

11:20am **PS-TuM11 Underlayer Impact on Line Width Roughness in Extreme Ultraviolet Lithography and Etch**, ***Indira Seshadri***, *A. DeSilva, Y. Mignot, W. Xu, L. Meli, J. Guo, S. Sieg, J.C. Arnold, N. Felix*, IBM Research Division

Extreme ultraviolet (EUV) lithography enables single expose patterning of fine-pitch features, eliminating the need for complex multiple patterning schemes. However, reduction of line width/line edge roughness (LER/LWR) to match multiple patterning is a fundamental challenge with EUV. Typical EUV patterning stacks consist of resist, hardmask and planarizing organic layer, and reduction of both the post-lithography resist LWR and the post hardmask etch LWR are key to achieving final feature targets. With EUV eliminating the requirement for reflectivity control, hardmask materials may be chosen based on high etch selectivity to resists, stack aspect ratio reduction and low defectivity (eg. Si-containing films). However, recent work[1,2] has shown that hardmask choice can significantly impact fundamental aspects of the lithography that are strongly correlated to LER/LWR, such as dose, process window and EUV secondary electron capture through interactions at the resist-hardmask interface. Here, we demonstrate the impact of different classes of hardmask materials on LWR in fine pitch metal line features, post litho and post etch. With three classes of hardmasks – Organic spin-on films, inorganic deposited Si-based films, and metal containing films, we first evaluate post lithography LWR with low and high sensitivity resists and dipole and quadrupole illumination shapes. We then characterize LWR after under layer open with optimal etch chemistries to reach target line/space sizes. With frequency analysis of LWR[3], we present fundamental mechanisms that explain the LWR trends arising from resist-illumination-hardmask interaction and etch based LWR smoothing for each class. Our results provide a key knob to aid hardmask selection to meet LWR targets for future nodes

1. A. DeSilva, I. Seshadri, A. Arceo, K. Petrillo, L. Meli, B. Mendoza, Y. Yao, M. Belyansky, S. Halle, N. Felix, "Study of Alternate hardmasks for extreme ultraviolet patterning", J. Vac. Sci. Technol. B 36 (6), 2016.

2. D. De Simone, Y. Vesters,A. Shehzad, G. Vandenberghe, P. Foubert, C. Beral, D. Van den Heuvel M. Mao, F. Lazzarino, "Exploring the readiness of EUV photo materials for patterning advanced technology nodes," Proc. SPIE 10143 (2017).

3. R. Bonam, C. Liu, M. Breton, S. Sieg, I. Seshadri, N. Saulnier, J. Shearer, R. Muthinti, R. Patlolla, H. Huang," Comprehensive analysis of line-edge and line-width roughness for EUV lithography", Proc. SPIE 10143 (2017).

11:40am **PS-TuM12 Patterning Challenges and Perspective Solutions for 5nm and Beyond**, ***Ying Zhang***, Applied Materials, Inc. **INVITED**

Patterning has imposed new challenges and opportunities to Etch, Film metrology. In a variety of multiple patterning schemes, such as Multiple Litho + Etch (LELE…), or Self-Aligned Multiple Patterning (SAxP), Edge Replacement Error (EPE) is approaching the limit, ~¼ of pitch, which will limit the continuing of pitch shrink [1]. The recent development of EUV technology and manufacturability will help to realize much needed complementary lithography technology [2]. The challenges of reducing EPE (< e.g., ~ ¼ pitch), pitch walking, and CD/CDU/LER/LWR controllability in <0.5 nm (3s) regime have shifted from Lithography to Films, Etch and Metrology. Continuous improvements of current plasma etch and film technologies are facing challenges to carry out the tasks of multiple patterning for the industry to extend to 5nm. Can process fine tuning based on current plasma etch and film tool technologies accomplish the precision requirement of fabricating sub-20nm pitch patterning? Atomic Layer Deposition (ALD) technology has already played a key in self-aligned multiple patterning. Further exploring on ALD and gapfill technology to provide more films with conformal and gapfill capabilities are required to enable some highly challenging patterning schemes. Conceptually, Atomic Layer Etching (ALE) should be able to help, e.g., CD control, etch selectivity, etc. But the key question is how to realize true ALE. In this talk, some of the new developments, key challenges, and perspective solutions on processes, process integrations, and plasma etching and film systems for will be reviewed and discussed.

[1] Richard Schenker, Intel, SPIE 2016, Feb, 2016, San Jose, USA

[2] Yan Borodovsky, Intel, Leti Innovation Days, June 26th 2013, Grenoble, France

Authors Index
Bold page numbers indicate the presenter

— A —

Arnold, J.C.: PS-TuM11, 2

— B —

Bi, Z.: PS-TuM1, 1
Biolsi, P.: PS-TuM2, 1

— C —

Canaperi, D.: PS-TuM1, 1

— D —

DeSilva, A.: PS-TuM11, 2
Devarajan, T.: PS-TuM1, **1**
Devries, S.: PS-TuM1, 1

— F —

Felix, N.: PS-TuM11, 2
Fukasawa, M.: PS-TuM5, 2

— G —

Greene, A.: PS-TuM1, 1
Guo, J.: PS-TuM11, 2

— I —

Ishii, Y.: PS-TuM3, **1**

— J —

Joy, N.: PS-TuM2, **1**

— K —

Kuboi, N.: PS-TuM5, **2**

— L —

Loubet, N.: PS-TuM1, 1

— M —

Maeda, K.: PS-TuM3, 1
Manos, J.: PS-TuM3, 1
Meli, L.: PS-TuM11, 2
Miao, B.: PS-TuM1, 1
Mignot, Y.: PS-TuM11, 2

— O —

Okuma, K.: PS-TuM3, 1

— P —

Peck, J.A.: PS-TuM4, **1**

— R —

Ranjan, A.: PS-TuM2, 1
Ruzic, D.N.: PS-TuM4, 1

— S —

Scott-McCabe, R.: PS-TuM3, 1
Sebastian, J.: PS-TuM3, 1
Seshadri, I.P.: PS-TuM11, **2**
Sieg, S.: PS-TuM11, 2
Strane, J.: PS-TuM1, 1
Surisetty, C.: PS-TuM1, 1

— T —

Tatsumi, T.: PS-TuM5, 2

— V —

Voronin, S.A.: PS-TuM2, 1

— W —

Walker, M.: PS-TuM3, 1
Wang, M.: PS-TuM1, 1

— X —

Xu, W.: PS-TuM11, 2

— Y —

Yao, Y.: PS-TuM1, 1
Yeung, C.: PS-TuM1, 1
Young, L.: PS-TuM1, 1
Yu, A.: PS-TuM3, 1

— Z —

Zhang, J.: PS-TuM1, 1
Zhang, Y.: PS-TuM12, **2**
Zhou, H.: PS-TuM1, 1