2D Materials Focus Topic
Room: 16 - Session 2D+EM+MN+NS-WeA

2D Device Physics and Applications
Moderator: Humberto Gutierrez, University of South Florida

2:20pm **2D+EM+MN+NS-WeA1 Capacitance-voltage Characteristics of Graphene-gate MOS Devices: The Effect of Graphene Quantum Capacitance**, ***Ruixue Lian***, *A. Ural*, University of Florida

There has been significant research interest in graphene for electronics applications, due to its good electrical conductivity, high optical transparency, mechanical flexibility, and two-dimensional structure. However, the potential of graphene as a channel material replacing silicon is limited due to the absence of a bandgap. On the other hand, graphene is an excellent candidate as a transparent, conductive, and flexible electrode for electronic and optoelectronic devices.

Unlike conventional metals, whose Fermi level is typically pinned at the surface, the Fermi level and hence workfunction of graphene can be tailored by electrostatic gating, chemical doping, or surface engineering. As a result, graphene is also a promising candidate as the gate electrode in metal-oxide-semiconductor (MOS) devices, particularly when transparency or workfunction tunability is a requirement.

In real graphene sheets, charged impurities cause electron-hole puddles and random local electrostatic potential fluctuations (statistically described by a Gaussian distribution), which leads to a modified density of states (DOS). In this work, using this modified DOS, we numerically compute the quantum capacitance of graphene as a function of the graphene electrostatic potential at different temperatures and strengths of the potential energy fluctuations. We compare the exact results to various approximations made in the literature when fitting experimental data. We find that the largest discrepancy between the exact results and the approximations occurs near the Dirac point.

In capacitance-voltage (C-V) characterization of graphene-gate MOS devices, what is measured is not the quantum capacitance versus the graphene potential, but the total gate capacitance versus the gate voltage. We numerically compute the gate voltage as a function of the graphene potential and the resulting C-V characteristics at different temperatures, strengths of the potential energy fluctuations, and equivalent oxide thicknesses. We also consider the effect of series and parallel parasitic impedance to the overall shape of the C-V curves. Furthermore, we numerically compute the full C-V characteristics at different values of the equivalent oxide thickness, silicon doping density, and Dirac voltage of graphene. Finally, we fit our recent experimental C-V data with these theoretical calculations to extract the strength of the potential energy fluctuations and the parasitic impedances.

These results provide important insights into the effect of the graphene quantum capacitance on the C-V characteristics of MOS devices and the potential of graphene as a gate electrode in future MOS technology.

2:40pm **2D+EM+MN+NS-WeA2 *in-situ* Electrical Characterization of Surface Functionalization and Gate Dielectric Deposition Processes on 2D Transition Metal Dichalcogenides Transistors**, ***Antonio T. Lucero***, *J.B. Lee, L. Cheng, H.S. Kim, S.J. Kim, J. Kim*, University of Texas at Dallas

Two-dimensional transition metal dichalcogenide (TMD) materials are a subject of intense research for use as future, low-power semiconductors. The successful fabrication of TMD based transistors requires a scalable dielectric deposition process. Atomic layer deposition (ALD) is commonly used to grow high-k gate dielectrics, though deposition of thin, pin-hole free dielectrics is challenging due to the chemically inert basal plane of most TMD materials. To overcome this limitation, surface functionalization processes have been developed to improve ALD nucleation.

In order to elucidate the effects of surface functionalization and subsequent ALD on the electrical characteristics of TMD transistors we use an *in-situ* electrical characterization system to measure the electrical properties of TMD transistors at various steps during the deposition process. MoS_2 backgated transistors are loaded into an ultra-high vacuum (UHV) cluster tool where samples can be transferred under UHV conditions between various chambers. The cluster tool is equipped with a thermal ALD chamber, a hollow cathode plasma enhanced ALD chamber, a plasma enhanced chemical vapor deposition chamber, and a UHV electrical probe station. Results for ozone, nitrogen radical, and nitrogen plasma functionalization will be presented. The effect of surface dipoles, precursor adsorption and coverage, and nucleation during the ALD process will be discussed as they relate to the electrical characteristics of the device.

This work was supported by the SWAN Center, a SRC center sponsored by the Nanoelectronics Research Initiative and NIST, and by NRF (No. 2015M3D1A1068061) in Korea. We thank TMEIC for providing the ozone generator and nitrogen radical generator used in this work.

3:00pm **2D+EM+MN+NS-WeA3 High-K Gate oxide by Low Temperature ALD Technique for 2D Materials and Inert Metal Surfaces**, ***Il Jo Kwak***, *J.H. Park,* University of California at San Diego*, S. Fathipour, A. Seabaugh,* University of Notre Dame*, C.S. Pang, Z. Chen,* Purdue University*, A.C. Kummel*, University of California at San Diego

2D materials such as TMDs(Transition Metal Dichalcogenides), Graphene and BN have attracted great attention as new channel materials for future devices due to their excellent electronic and optical properties. For such devices, sub nanometer thick and defect free gate oxide is an essential part. However, due to the inert surface of the materials, high K oxide such as Al_2O_3 and HfO_2 selectively nucleates on defect sites or step edges. Therefore, for successful integration, preparation of uniform and insulating gate oxides are a matter of importance. In this study, Al_2O_3 was deposited on 2D materials surface by low temperature ALD using trimethylaluminum(TMA) and H_2O without any seeding layer or surface treatments. Using short purge time between two precursor pulses at 50C, a CVD component was induced to provide uniform nucleation sites on the surface. The CVD component generates subnanometer AlOx particles[s1] [file:///C:/Users/kwak1/Downloads/2017_AVS_abstract_bilayer_oxide.docx#_msocom_1] on the surface which provide uniform nucleation sites. In order to obtain lower EOT layer, 10 cycles of Al_2O_3 ALD was deposited at 50C as a seeding layer and 40 cycles of HfO_2 ALD was deposited with Tetrakis(dimethylamido)hafnium (TDMAH) and H_2O at 250C. The same oxide was deposited on a SiGe substrate to compare the oxide characteristics. After ALD, MOSCAPs were fabricated to measure electrical properties. AFM measurement revealed that uniform and defect free oxide layers were nucleated on the surfaces. Capacitance-voltage measurement showed that Cox of the bilayer oxide was 2.5 uF/cm2 and the gate leakage current of the oxide was about 10^{-5} A/cm^2 which was comparable to the oxide on a SiGe substrate. Identical bilayer oxide layer was deposited on a dual gated WSe_2 FETs . Top gate oxide leakage of the device was about 10^{-6} A/ cm2. In order to assess the quality of the oxide, a benchmarking study of current density versus EOT of 2D semiconductor FET devices and Si based devises was investigated. The study showed that record-low EOT (1.2 nm) and leakage current (10^{-8} μA/ μm^2) comparable to the best Si devices with La_2O_3 gate oxide by Iwai *et al* was achieved by the WSe2 FET. This technique was also applied to initiate nucleation[s2] [file:///C:/Users/kwak1/Downloads/2017_AVS_abstract_bilayer_oxide.docx#_msocom_2] on inert metal surfaces which are important for logic memory devices including selectors. Using the bilayer oxide, insulating oxide was prepared on Au electrodes of a MOSFET device. The leakage current of the oxide was as low as 10^{-7} A/ cm^2.

3:20pm **2D+EM+MN+NS-WeA4 Exploration and Comparison of Optoelectronic Properties of MoS_2 Monolayers with Multilayer Flakes and $Mo_xW_{1-x}S_2$ Ternary Compounds**, ***Sourav Garg***, *J. Waters, A. Mollah, S. Kim, P. Kung*, University of Alabama

2D transition metal dichalcogenide (TMDC) semiconductors, including MoS_2, WS_2, and more recently ternary compounds, exhibit exceptional structural, electrical and optical properties that make these materials of great interest for nano-optoelectronic devices. For example, unlike graphene, TMDCs have a bandgap, which has the remarkable characteristic of becoming direct when the material is in monolayer form, while it is indirect when the material is composed of multiple layers.

Here, we report the synthesis of monolayer MoS_2, WS_2, ternary $Mo_xW_{1-x}S_2$ ternary compounds and MoS_2/WS_2-based heterostructures, by chemical vapor deposition (CVD) process at temperatures in the range 950-1000 C, without the use of seeds to avoid contamination. The material was extensively characterized using micro-Raman spectroscopy, micro-photoluminescence, and electron microscopy.

Using such large area CVD grown materials, large-area MoS_2 photoconductive detector devices were fabricated using conventional photolithography to realize of interdigitated metal fingers. The electrical and spectral photoresponse from monolayer and multilayer MoS_2 have been compared, in terms of responsivity and specific detectivity. The monolayer devices exhibited high photoconductive gain and detectivity near 10^{12} Jones, which was also found to be higher than in the case of multilayer MoS_2 devices. The rise and decay time of passivated monolayer devices was investigated and shown to be much faster than the unpassivated devices.

4:40pm **2D+EM+MN+NS-WeA8 Dielectric Properties of Carbon Nanomembranes prepared from aromatic Self-Assembled Monolayers investigated by Impedance Spectroscopy**, ***Paul Penner***, *E. Marschewski, X. Zhang,* Bielefeld University, Germany, *T. Weimann, P. Hinze,* Physikalisch-Technische Bundesanstalt, Germany, *A. Beyer, A. Gölzhäuser*, Bielefeld University, Germany

Carbon nanomembranes (CNMs) are two-dimensional materials made by cross-linking self-assembled monolayers (SAMs) of aromatic molecules via low energy electron irradiation. Previous study of molecular junction incorporating SAMs and CNMs of oligophenyl thiols has been carried out by using conical eutectic Gallium-Indium (EGaIn) top-electrodes[1] and conductive probe atomic force microscopy (CP-AFM). Here we investigate the dielectric properties of pristine SAMs and CNMs with an EGaIn top electrode by impedance spectroscopy. Analysis and comparison of the tunneling resistance and capacitance density of pristine and cross-linked SAMs revealed a thickness dependent capacitance associated with the monolayer as well as a thickness independent capacitance. We adopted an equivalent circuit to take into account the contribution of the interfacial capacitance as well as the oxide layer of the EGaIn top electrode. The obtained tunneling decay constant remains unaffected after electron irradiation, which exhibits a value of about 0.5 $Å^{-1}$ for both systems. A determination of dielectric constants of SAMs and CNMs from the impedance spectra will also be analyzed and discussed. Furthermore we characterize stacks of CNMs sandwiched with graphene and other 2D materials.

[1] P. Penner, X. Zhang, E. Marschewski, et. al, J Phys Chem C 2014, 118, 21687.

5:00pm **2D+EM+MN+NS-WeA9 2D Crystals for Next-Generation Ultra Energy-Efficient Electronics**, ***Kaustav Banerjee***, University of California at Santa Barbara **INVITED**

I will highlight the prospects of two-dimensional (2D) materials for innovating energy-efficient transistors, sensors, and interconnects targeted for next-generation electronics needed to support the emerging paradigm of the *Internet of Things*. More specifically, I will bring forward a few applications uniquely enabled by 2D materials and their heterostructures that have been demonstrated in my lab for realizing ultra-energy-efficient electronics. This will include the world's first 2D-channel band-to-band tunneling transistor that overcomes a fundamental power consumption challenge in all electronic devices since the invention of the first transistor in 1947 (Nature 2015), as well as a breakthrough interconnect technology based on doped-graphene-nanoribbons, which overcomes the fundamental limitations of conventional metals and provides an attractive pathway toward a low-power and highly reliable interconnect technology for next-generation integrated circuits (Nano Letters 2016). I will also bring forward a new class of ultra-sensitive and low-power sensors as well as area-efficient and high-performance passive devices, both enabled by 2D materials, for ubiquitous sensing and connectivity to improve quality of life.

Authors Index

Bold page numbers indicate the presenter

— B —
Banerjee, K.: 2D+EM+MN+NS-WeA9, **2**
Beyer, A.: 2D+EM+MN+NS-WeA8, 2
— C —
Chen, Z.: 2D+EM+MN+NS-WeA3, 1
Cheng, L.: 2D+EM+MN+NS-WeA2, 1
— F —
Fathipour, S.: 2D+EM+MN+NS-WeA3, 1
— G —
Garg, S.: 2D+EM+MN+NS-WeA4, **1**
Gölzhäuser, A.: 2D+EM+MN+NS-WeA8, 2
— H —
Hinze, P.: 2D+EM+MN+NS-WeA8, 2
— K —
Kim, H.S.: 2D+EM+MN+NS-WeA2, 1
Kim, J.: 2D+EM+MN+NS-WeA2, 1
Kim, S.: 2D+EM+MN+NS-WeA4, 1
Kim, S.J.: 2D+EM+MN+NS-WeA2, 1
Kummel, A.C.: 2D+EM+MN+NS-WeA3, 1
Kung, P.: 2D+EM+MN+NS-WeA4, 1
Kwak, I.J.: 2D+EM+MN+NS-WeA3, **1**
— L —
Lee, J.B.: 2D+EM+MN+NS-WeA2, 1
Lian, R.: 2D+EM+MN+NS-WeA1, **1**
Lucero, A.T.: 2D+EM+MN+NS-WeA2, **1**
— M —
Marschewski, E.: 2D+EM+MN+NS-WeA8, 2
Mollah, A.: 2D+EM+MN+NS-WeA4, 1
— P —
Pang, C.S.: 2D+EM+MN+NS-WeA3, 1
Park, J.H.: 2D+EM+MN+NS-WeA3, 1
Penner, P.: 2D+EM+MN+NS-WeA8, **2**
— S —
Seabaugh, A.: 2D+EM+MN+NS-WeA3, 1
— U —
Ural, A.: 2D+EM+MN+NS-WeA1, 1
— W —
Waters, J.: 2D+EM+MN+NS-WeA4, 1
Weimann, T.: 2D+EM+MN+NS-WeA8, 2
— Z —
Zhang, X.: 2D+EM+MN+NS-WeA8, 2