Wednesday Afternoon, November 12, 2014

Selective Deposition as an Enabler of Self-Alignment
Focus Topic
Room: 318 - Session SD-WeA

Process Development for Selective Deposition and Self-Aligned Patterning

Moderator: Paul Ma, Applied Materials, Inc., John Smythe, Micron Technology

2:20pm **SD-WeA1 Material Requirements for Self-Aligned Patterning – a Lithographer's Perspective**, ***Charles Wallace***, Intel Corporation **INVITED**

As feature sizes shrink in semiconductor processes, overlay control is quickly becoming the most significant source of variation. Physical limitations of lithography equipment are constantly pushed beyond their capability in order to meet device requirements. This presentation will discuss past, current and future methods of decreasing overlay and critical dimension errors using self-alignment and selectivity. Self-aligned processes in logic-product manufacturing reduce edge-placement-errors (EPE) which improve yield and device performance. Self-aligned VIAs, self-aligned double patterning (SADP) and directed self-assembly (DSA) are some recent examples of complementary patterning techniques to conventional lithography. These processes enable scaling beyond the resolution limits of conventional lithography. In addition to addressing fundamental physical limitations of optical lithography, these techniques can help to reduce costs because of shorter patterning process flows and the use less expensive equipment. Now is the time for material design and selectivity (selective etch, deposition and removal) to start playing a major role in patterning in order to reduce and eliminate overlay error.

3:00pm **SD-WeA3 Controlling Selective Area Atomic Layer Deposition of Metals and Metal Oxides without the use of Organic Blocking Layers**, ***Gregory Parsons***, *B. Kalanyan, S.E. Atanasov*, North Carolina State University **INVITED**

Selective area CVD has been heavily studied, and several strategies for selective growth are known, including sacrificial reactions, surface activation, nucleating species removal and passivation of non-growth surfaces. However, the success of selective deposition processes in manufacturing has been limited. Atomic layer deposition allows the partial pressure and exposure sequence of individual reactants to be independently adjusted, providing additional control in surface reaction sequence. Surface passivation layers can promote selective area ALD of metals and dielectrics, but integration into manufacturing can be a challenge. Recently, we have studied modified ALD process sequences as a means to control nucleation, without the need for pre-deposited nucleation blocking layers. For example, tungsten ALD using WF_6/SiH_4 onto SiO_2 proceeds when surface Si-H (from SiH_4) begins to form, allowing WF_6 reduction to W and elimination of SiF_4. We hypothesized that the introduction of a H_2 or H-plasma exposure into the ALD sequence after the SiH_4 dose may help remove Si from the SiO_2, which could extend the nucleation delay on SiO_2, while not affecting W growth on Si. Using ellipsometry, XPS, high resolution SEM and in-situ quadrupole mass spectrometry we found that a H_2 exposure step after SiH_4 during W ALD on ex-situ prepared SiO_2 decreased the rate of W nucleation compared to growth without the H_2 step, effectively increasing the selectivity window. At 220°C, one ALD cycle produced nm-scale nuclei on Si-H surfaces, and film coalescence after ~10 cycles, whereas growth on SiO_2 showed no W nuclei after 10 cycles. After some nucleation, growth proceeded readily on the nuclei, with few new nuclei forming, producing rough surfaces that coalesced after 40 cycles. Including the H_2 exposure step after SiH_4 delayed nucleation by 5-10 cycles on SiO_2, with no noticeable effect on Si-H. However, we found that removing surface carbon from the SiO_2 prior to growth had a similar effect, indicating that C helped aid nucleation. Recent work with H_2-plasma exposure also shows enhanced nucleation on SiO_2, which likely depends on the extent of H exposure. In other studies, we are examining metal oxide nucleation using metal/metal alkoxide reaction sequences and comparing to similar reactions with water as a reactant. These results will help to define ALD nucleation sequences that are distinct from steady-state film growth, to achieve reliable selective area deposition.

4:20pm **SD-WeA7 Selective Deposition through Organic Blocking Layers**, ***Rami Hourani***, *S.B. Clendenning, G.M. Kloster, A. Basu, F. Gstrein*, Intel Corporation

With the ever increasing complexity of lithography and associated patterning techniques, pattern overlay has become a critical limiter for the continued scaling of integrated circuits. Self-alignment of patterns through area selective deposition, or area-selective etch is an attractive way of addressing pattern overlay and edge placement challenges. Inherently, surface-selective deposition techniques are rare in the fields of chemical vapor deposition (CVD) and atomic layer deposition (ALD). This is particularly true for the selective deposition of dielectrics. Tuning the chemical properties of precursors to achieve inherent substrate-dependent selectivity is thus a key enabler. In the face of poor inherent selectivity, using organic layers such as self-assembled monolayers (SAMs) as blocking layers for subsequent CVD and ALD deposition is an attractive way of achieving selective growth and controlling defectivity. In this paper we will present a joint experimental and theoretical investigation (Density Functional Theory based calculations with semi-empirical dispersion correction) aimed at assessing the stability of a variety of SAMs and their ability to block the deposition of a dielectric thin film. Simple line space patterns will be used to assess the defectivity of this approach. The critical parameters to achieve area-selective deposition will be discussed including proper surface pre-treatment, optimization of the SAM deposition through judicious choice of SAM terminal group and carbon chain length, and optimization of the deposition process through ALD precursor choice. Finally, obstacles to making selective deposition processes manufacturable will be discussed.

4:40pm **SD-WeA8 Selective Deposition and Selective Etching of Patterned Dielectric Films**, ***FatemehSadat Minaye Hashemi***, *C. Prasittichai, S.F. Bent*, Stanford University

Planar and 3-D electronic structures such as those found in FinFETs contain metal/dielectric patterns, for which selective deposition processes may facilitate the fabrication of device features on the length scale of nanometers. The ultimate adoption of selective deposition approaches in device fabrication will require a technique that can provide for deposition of different materials with a variety of thicknesses while maintaining the selectivity even at high thickness limits. Atomic layer deposition (ALD) is a good choice for selective deposition because it is based on self-limiting reactions between gas phase precursors and specific functional groups at the growth surface. This chemical specificity provides a means to achieve selectivity in ALD on a spatially patterned substrate.

In our previous studies, we have demonstrated area selective ALD of dielectric-on-dielectric by selectively depositing an organic self-assembled monolayer (SAM) of octadecylphosphonic acid (ODPA) as the blocking layer on metal parts of a metal/dielectric (Cu/SiO_2) pattern. This approach provided the ability to carry out selective deposition for film thicknesses above 10 nm. However, the deposition time of a well-packed ODPA passivation layer required to achieve such selectivity was over 40 hours. Also, it is desirable to remove the organic ODPA molecules from the metal surface after the process of area selective ALD. Moreover, due to the diverse chemical nature of different dielectric precursors, when using very reactive precursors the selectivity achieved using an ODPA passivation layer can be limited to dielectric film with thicknesses less than 10 nm. Here we propose a new strategy to resolve these issues by performing selective deposition combined with selective etching of dielectric films on metal/dielectric pattern.

In this approach, we first selectively deposit ODPA SAMs on a Cu/SiO_2 pattern for a reduced deposition time. Subsequent ALD processes of dielectric material on the substrate results in poor or no selective deposition on the substrates. Then we use a mild etchant to selectively remove the deposited dielectric film on Cu surface without affecting the film grown on neighboring SiO_2. X-ray photoelectron spectroscopy (XPS) and Auger electron spectroscopy (AES) measured after applying the etchant confirm no residual dielectric film on Cu, while ellipsometry and XPS results show metal oxide growth on SiO_2. We thus show that using this method, not only the area selective ALD is achievable with more rapid processing but also high selectivity can be reached for deposition of a variety of high-κ dielectric materials, opening up the possibility for ne w applications.

5:00pm **SD-WeA9 All-Dry Etching Strategy for Self-Assembly Block Copolymers PS-b-PMMA**, ***Philippe Bézard***, *G. Cunge, E. Latu-Romain, A. Tavernier,* LTM, France, *R. Tiron,* CEA-LETI, France, *X. Chevalier,* Arkema, France, *O. Joubert*, LTM - CEA/LETI, France

Vertically aligned cylinder block copolymers are often considered to be used as etching masks for hole patterning with very aggressive critical

dimensions (CD) – typically sub-15nm. PS-b-PMMA, as a di-block copolymers configuration, has been thoroughly studied in the past decade [1]. The transfer strategy with PS-b-PMMA features [2] is to remove PMMA by wet or dry processes and to use PS as a mask for etching. A combination of UV and acetic acid bath has shown good results [3] but requires several specific steps as PMMA residues removal in addition to brush layer [4] and hard mask opening. An all-dry strategy would consist of trading three steps (UV, wet, PMMA residues plasma etching) with a single PMMA cylinder etching one without additional CD dispersion, providing a substantial process flow simplification for industrial purpose.

A deep understanding of both PMMA and PS etching mechanisms under various plasma conditions in terms of chemistry and ion energy is then required to overcome this challenge. Rigorous material- and plasma characterisations lead to the use of H2-based plasma chemistry rather than O2-based plasmas. Conventional oxygen-based plasmas result indeed in a poor selectivity (around 2) due to similar material composition, leading to CD degradation. Selectivity in H2-based plasma benefits from PMMA-exclusive C-O and C=O bonds which are easily broken (weakening the material) when PMMA is exposed to H2 (as evidenced by XPS and MIR results).

We will present results obtained both in synchronously-pulsed [5] and continuous wave low pressure Inductively Coupled Plasmas (ICP) in H2-based chemistry. While synchronously-pulsed ICP plasmas allow efficient brush layer opening [3], best selectivity is achieved in continuous wave ICP plasmas.

As a result, transfer of sub-15nm 60nm-deep nanoholes into silicon with about 2nm CD dispersion has been achieved without using any hard mask strategy.

[1] K.W. Guarini &al., J. Vac. Sci. Technol. B **19**, 2784 (2001)

[2] R.Tiron &al., Proc. SPIE 8680, Alternative Lithographic Technologies **V**, 868012 (2013)

[3] P.Bezard &al., Plasma etching of sub-14nm holes in silicon using PS-b-PMMA block-copolymer masks, PESM (2014)

[4] X.Chevalier &al., Proc. SPIE 8680, Alternative Lithographic Technologies **V**, 868006 (2013)

[5] S.Banna &al., Journal of Vacuum Science & Technology A **30**, 040801 (2012)

5:20pm **SD-WeA10 Selective CVD Cobalt Capping Advanced-Groundrule Cu Interconnects : Electromigration Study**, ***Andrew Simon***, IBM Microelectronics Division, *T. Bolom,* GLOBALFOUNDRIES Inc., *C. Niu,* ST Microelectronics, *F.H. Baumann,* IBM Microelectronics Division, *C.-K. Hu,* IBM Research Division, *C. Parks, J. Nag,* IBM Microelectronics Division, *J.-Y. Lee,* GLOBALFOUNDRIES Inc., *C.-C. Yang, S. Nguyen,* IBM Research Division, *D. Priyadarshini, D. Kioussis,* IBM Microelectronics Division, *T. Nogami,* IBM Research Division, *S. Guggilla, J. Ren, J. AuBuchon*, Applied Materials, Inc.

A key requirement in scaling of Cu interconnects to groundrules at 14nm is maintaining electromigration (EM) performance. Adhesion of the Cu to the capping layer is a major reliability limitation, and adhesion-promotion schemes involving self-segregation of alloy components (e.g., Al, Mn) and selective metal capping (most often Co) have been developed. A parallel development is the use of seed-enhancement liner layers, (e.g. CVD Co), to improve conformality and Cu wettability while maintaining compatibility with established polishing processes. In this study, we compare the EM performance of CuMn self-capping to selective CVD Co capping on 22nm-Groundrule Cu interconnects, with and without the use of a CVD Co seed-enhancement layer.

Dual-damascene 22nm-groundrule interconnects were etched in a k=2.5 dielectric. Deposition of the PVD Ta(N) barrier, CVD Co liner layer and PVD Cu or CuMn seed layers was done on a clustered mainframe. After plating and CMP, capping was done either with $SiC_xN_yH_z$ alone, or with selective CVD-Co followed by $SiC_xN_yH_z$.

SIMS studies [1] comparing Mn-depth profiles of CuMn-seeded samples with a PVD Ta(N)-only liner vs a Ta(N)/CVD Co liner were done on wires capped only with $SiC_xN_yH_z$. The PVD TaN/Ta liner shows a spike in Mn-concentration at the cap-layer interface of ~8e20 atoms/cm^3, consistent with enhanced EM. In contrast, the CVD Co seed-enhancement layer results in a ~5x suppression of Mn self-capping due to the presence of the carbonyl CVD Co layer (Fig.1).

Further studies compared PVD TaN/Ta liner / CuMn seed samples vs. selective CVD Co capped-samples with either (a) PVD TaN/Ta / Cu seed -or- (b) PVD Ta(N) / CVD Co-liner / PVD Cu liner/seed schemes. Fig. 2 shows TEM/EDX images of selective-CVD Co capped samples with both PVD Ta(N)-only or PVD Ta(N) / CVD Co liners. The full-encapsulation of the Cu wire with the CVD Co liner and selective CVD Co cap is apparent in the lower-right EDX image, with strong Co signals around the entire periphery. In contrast, the sample with Co only in the selective capping layer (upper right) shows a strong Co signal only in the cap layer.

Median downstream EM lifetimes at 300C for PVD Ta(N)/ Liners with either Co caps or CuMn seedlayers were in the range of 15-40 hours (Fig.3), consistent with previously-reported activation energies of 1.0eV[2]. However, the CVD Co Liner / selective Co cap samples showed median failure times of >150 hours at 400C and >3000 hours at 340C (Fig. 4), indicating an exceptionally high activation energy of 1.7 eV. **Acknowledgements:** This work was performed by the Research and Development Alliance Teams at various IBM Research and Development Facilities

5:40pm **SD-WeA11 Growth and Characterization of Ultra-Thin Silicon Dioxide Layers for Low-k Dielectrics on HOPG and Graphene**, ***Antonio Lucero***, *L. Cheng, Y.G. Lee, HH. Hwang, X. Qin, R.M. Wallace, J.Y. Kim*, University of Texas at Dallas

Despite graphene's excellent electrical properties, little progress has been made in developing a successful, high performance logic device due to the difficulty of creating a band gap. A proposed device which side steps this issue is the graphene bilayer pseudo-spin field effect transistor (BiSFET)[1]. It has been suggested that a low-k, ultra-thin (<3 nm) tunneling dielectric is needed for the operation of the BiSFET. The inert surface of graphene presents challenges for the scaling that is necessary to grow this ultra-thin layer. This work focuses on the development of a SiO_2 deposition process which can be used as a low-k tunneling barrier. Additionally, we investigate the inclusion self-assembling monolayers (SAM) to further reduce the dielectric constant. To this aim, two growth techniques well-known for their thin film growth capabilities are compared: molecular beam epitaxy (MBE) and atomic layer deposition (ALD).

Growth using MBE and ALD is studied on both highly ordered pyrolytic graphite (HOPG) and transferred graphene. For MBE growth, silicon deposition is carried out in a UHV cluster tool and the films are subsequently oxidized to form SiO_2. Film growth has been scaled from 3 to 1 nm in thickness while maintaining uniform coverage. The ALD process uses tris(dimethylamino)silane and ozone at room temperature for growth. *In-situ* static ozone treatment is used to encourage nucleation similar to previous work [2]. The static ozone cycle is repeated from 3 to 10 times in order to study the scalability of the process. Thickness varies from 2 to ~1 nm, depending on the number of cycles. Growth rate is calculated using x-ray photoelectron spectroscopy (XPS) attenuation of substrate peaks and confirmed with transmission electron microscope. Surface morphology is intensively studied using an atomic force microscope (AFM) to ensure films are continuous and uniform. Morphology for MBE and ALD films is good even when scaled to 1 nm. Raman spectroscopy confirms that no significant defects form during the growth process. Metal-insulator-metal (MIM) capacitors are fabricated in order to evaluate the effectiveness of the ultra-thin silicon dioxide films as tunneling dielectrics both as-is and with octadecyltrichlorosilane SAM functionalization. Results indicate that both MBE and ALD SiO_2 are effective tunneling dielectrics with and without OTS.

We would like to thank the Toshiba Mitsubishi-Electric Industrial Systems Corporation (TMEIC) for providing the ozone generator used in this study and SWAN for their financial support.

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