Plasma Science and Technology
Room: 308 - Session PS-MoM

Current Challenges of Plasma Etching Technologies

Moderator: Saravanapriyan Sriraman, Lam Research Corp

8:20am **PS-MoM1 Dielectric Etch Challenges and Evolutions**, ***Masanobu Honda***, Tokyo Electron Miyagi Limited, Japan **INVITED**

For 7nm and beyond VLSI nano fabrication, fine process control in the order of nm or less is required, current incremental techniques may not address the challenges for future nano fabrication. In the High Aspect ratio processing such as 3DNAND and DRAM capacitor, miniaturization of the feature dimensions adds challenges to ion-radical transportation to the bottom of the feature, further aggravating etch yield and etch linearity. Further, in Logic MOL SAC, trade-off between the etch linearity and substrate recesses reduction are increasingly being focused. On the other hand, for BEOL interconnects, achievement of within-wafer uniformity of nm or less, and defect reduction at fine-node are added challenges. We have continued to challenge a variety of these dielectric etch issues, in order to provide technical solutions to enable future devices.

With further lithography related challenges and delays, complexity in patterning increases etch related challenges, continuous processing of the multilayer film with high accuracy corresponding to the multi-pattern is required. ARDE, reducing line roughness (LER/LWR), Trim, Hole Shrink and countermeasures in accordance with the thinning of the EUV resist are important challenges that etch has to overcome. We have effectively overcome these problems using unique resist treatment technologies based on high-speed electron beam and a sidewall protection film using DC super-imposed RF plasma system [1,2]. However, we still encounter trade-off when solving these challenges, it is necessary to overcome the trade-off by introducing a new concept to enable further miniaturization.

As noted above, there are many challenges and potential tradeoffs to arrive at an optimal solution; we need a breakthrough to overcome these challenges. We have continued to explore and innovate solutions, as a result we are honing on a possible solution integrating etch and ALD techniques. Establishing this Etch-ALD concept and developing a robust flow will be a major breakthrough in overcoming patterning and other critical level issues related to nano-feature processing dielectrics and to sustain the Moore's Law.

Reference

[1] M. Honda et al., AVS 60th Int. Symp. & Exhibit. (2013)

[2] M. Honda et al., Proc. of SPIE 8328-09 (2012)

9:00am **PS-MoM3 Improving Selectivity for 10nm BEOL Etch Using C5HF7 Gas**, ***Robert Bruce***, IBM T.J. Watson Research Center, *T. Suzuki, M. Nakamura*, ZEON Chemicals L.P., *A. Itou, G. Matsuura*, Zeon Corporation, *S.U. Engelmann, N.P. Marchack, E.M. Sikorski*, IBM T.J. Watson Research Center, *J. Lee*, IBM Albany Nanotech Center, *E.A. Joseph*, IBM T.J. Watson Research Center

As the industry moves to the 10nm technology node and beyond, new plasma etch challenges arise in the fabrication of back-end-of-line (BEOL) interconnects that need to be overcome. New materials and ever smaller critical dimensions require superior performance in etch, especially in minimizing line-edge roughness and low-k dielectric damage and improving hard mask selectivity. During dual damascene trench etch, low-k plasma damage leads to an increase in dielectric constant and pattern collapse. Also, during the self-aligned via (SAV) etch, vias short between one another due to poor metal hard mask selectivity and merging from via to via. Incorporating C5HF7 gas in these etch processes has shown significant improvements overall, because of its selective deposition properties. However, the C5HF7-based etch process needs to be tuned for the specific application, such as superior TiN selectivity for SAV or SiN selectivity for contact etch. In this talk, the optimized C5HF7-based processes for trench, SAV and contact are reviewed and compared. Furthermore, fundamental learning is accomplished using optical emission spectroscopy and x-ray photoelectron spectroscopy to understand the differences in mechanism between the various process regimes.

9:20am **PS-MoM4 Effect of 147nm Photons on Porous Organo-Silicon Glass Materials and Damage Improvement by Optimized Cu/Low-k Integration Approaches**, *L. Zhang*, IMEC, KU Leuven, Belgium, ***Jean-Francois de Marneffe***, IMEC, Belgium, *M. Lukaszewicz*, Wroclaw University of Technology, Poland, *S. Barry-Porter, F. Vajda*, Trinity College Dublin, Ireland, *Y. Sun*, IMEC, Belgium, *M.H. Heyne*, IMEC, KU Leuven, Belgium, *M. Baklanov*, IMEC, Belgium

Porous organo-Silicon glass thin films, with porosities ranging from 8 to 48% and k-values from 2.7 to 1.9 were exposed to 147nm photons and ions emitted in a CCP discharge of Xe. The material changes have been measured by means of various surface and bulk analytical techniques. For high-porosity/low k-value, a strong Si-CH_3 depletion is observed, concomitant with moisture and increase of silanol group density. Surface densification occurs, as well as reduction of porosity. TOF-SIMS elemental profile indicate however that C and O profiles stay rather constant through the film thickness, only slightly changing in absolute value. Change of material properties are reflected in a rapid increase of the bulk dielectric constant. It is observed that 147nm VUV photons dissociate Si-C bonds, releasing -CH_3 and other H-based radicals in the porous matrix, reacting with dangling Si* and forming Si-H. It is shown that Si-H bonds are also dissociated by VUV but their loss is compensated until -CH_3 are completely dissociated. In absence of reactant to form volatile compound with, a major part of those radicals form complex polymers that condensate into the pores, while, upon ambient exposure, moisture react with remaining Si-dangling bonds forming highly polarizable silanol groups. The impact of VUV exposure on low-k dielectrics with varying porosities indicate a direct correlation between absolute Si-CH_3 loss and VUV dose, independent of inital methyl bond density. Change in dielectric properties (k-value) follows the same trend, showing, at fixed VUV dose, a dielectric shift $\Delta k = 1.0$ independent of the pristine k-value.

The observed trend suggest that, besides reactive radical diffusion, photons emitted during plasma processing do severely impede dielectric properties, and therefore need to be tackled appropriately during patterning and integration.

In order to reduce the impact of VUV, hardmasks with high photon absorption and the effect of polymer filling by the P4 or 'pore stuffing' approach were evaluated. Several mask materials were deposited on top of blanket OSG 2.0 low-k films and exposed to 147nm photons. Various polymers with different UV absorption properties were stuffed into porous OSG 2.0 low-k films and then exposed to 147nm photons. For both cases, low-k damage was evaluated and showed reduced VUV damage.

9:40am **PS-MoM5 Non-PFC Plasma Chemistries for Patterning Low-k Dielectric Materials**, ***Jack Kun-Chieh Chen***, *N. Altieri, M. Paine, T. Kim, J.P. Chang*, UCLA

Low-k materials, such as fluorine-doped and carbon-doped silicon dioxide, exhibit reduced dielectric constants necessary to curtail parasitic capacitance and avoid crosstalk in devices, keeping pace with the trend of increasing device densities. SF_6 and perfluorocarbons (PFC) gases, which are primarily used in plasma etch of interlayer dielectric materials, generally have high global warming potentials (GWP), making their increased usage undesirable. This work focuses on evaluating etch chemistries from a thermodynamic standpoint for back end of line (BEOL) applications in patterning of proposed low-k carbon-doped silica compounds with varying carbon content. Group and bond additivity methods were used to estimate the Gibbs free energies of formation for these carbon-doped compounds. PFC and non-PFC etchants with H_2/NH_3 were assessed through the use of volatility diagrams comparing partial pressures of volatile etch products as a function of etchant partial pressure at 300K. Minimization of Gibbs free energy was employed to calculate the equilibrium distribution of species in the etch system across a range of temperatures. NF_3 and CF_3I were identified as potentially viable for etching carbon-doped silica. NF_3, a non-PFC gas with an atmospheric presence of 1ppt, GWP of 16,800, and much greater abatement efficacy, is the most effective etchant in pure form, producing volatile etch product pressures between six and eight times that produced by CF_4. CF_3I, despite being an iodofluorocarbon gas, exhibited a GWP of unity and displays reduced damage to doped carbon, making it preferable in etching carbon-doped silica. Pure CF_3I shows reduced product pressure with increasing carbon content; however, addition of H_2 and NH_3 improves its performance for the three most highly doped silica compounds. Given the higher cost associated with using NF_3 and CF_3I, the introduction of an additive (H_2 or NH_3) was assessed. Addition of H_2 and NH_3 generally showed an increase in partial pressures predicted by the volatility diagrams, with H_2 producing a much more significant increase than the pure etchant or the addition of NH_3. Preliminary experimental results comparing etch rates for moderately to highly carbon-doped silica samples with 20 sccm CF_4 and

hydrogen addition generally agree with theorized predictions. Varying the feed composition between 0%, 20%, and 50% H_2, etch rates of 38.2, 44.8 and 48.86 nm/min were recorded for lightly doped silica, and 49.2, 73.0 and 128.2 nm/min were recorded for heavily carbon-doped silica.

10:00am **PS-MoM6 Optimization of the Optical Transmission of Submicron Silicon-on-Insulator Rib Waveguides**, ***Marc Fouchier***, *E. Pargon,* CNRS/UJF/CEA-LTM, France, *B. Ben Bakir, P. Brianceau, J. Harduin, S. Barnola, P. Grosse*, CEA-LETI, France

Optical interconnects have largely replaced copper for long distance data transmission and are gaining interest on shorter distances. At the intra-chip level, silicon waveguides are foreseen to relieve copper wire bottlenecks in the BEOL layers. The strong light confinement allowed by the large refractive index difference between Si and SiO_2 permits the building of submicron silicon on insulator (SOI) waveguides with small bending radii and thus of compact photonic circuits. However, the strong light confinement also results in large propagation losses due to the scattering of the guided light on the rough etched sidewalls of the silicon core. Modeling shows that the transmission loss mostly depends on the line edge roughness (LER) of the guide and on its correlation length.

In the present work, we apply our silicon processing and sidewall roughness metrology know-how developed for transistor gates to optimize the fabrication process of submicron rib waveguides on 200 mm SOI wafer in order to reduce their optical loss. First SiO_2 and photoresist etch masks are evaluated. In both cases, the eventual benefit of an HBr plasma cure treatment, originally developed for FEOL processing, on the photoresist is also assessed. Second, we investigate the impact of several silicon smoothing strategies on the patterned waveguides: thermal oxidation and hydrogen annealing. Oxidations are performed in pure O_2 at 1000°C, above the SiO_2 viscous transition. The following thicknesses are tested: 5, 10, 30 and 3 × 10 nm. Oxidizing in three steps compared to a single longer step is believed to increase LER reduction because smoothing is faster in the initial reaction limited regime than in the subsequent diffusion limited regime. Hydrogen annealing is performed in pure H_2 for 2 min at several temperatures between 850 and 1000°C. After each process step the LER is measured by CD-SEM. In order to obtain LER values freed from instrumental noise and their correlation length, CD-SEM data are treated by spectral analysis . At the end of the process, the sidewall roughness of the rib waveguides is also characterized by AFM on a tilted sample. In addition, their profile is measured by cross-sectional SEM and their transmission loss on an optical test bench.

Measurements show that a resist mask is better than the SiO_2 mask for minimizing optical attenuation at the price of a degraded profile while the photoresist cure treatment does not have much influence. Further experiments are ongoing to evaluate the impact of the silicon smoothing processes (hydrogen annealing or thermal oxidation) on the roughness and to correlate it with optical loss measurements.

10:40am **PS-MoM8 Using Post Etch Treatment (PET) to Resolve Poly Residue Defect Issue of Dummy Poly Removal (DPR) in hi-K Metal Gate Processing**, ***Chih-Chien Wang***, *F.Y. Chang, C. Li-Chiang, S.-Y. Lu,* United Microelectronics Co., Taiwan, Republic of China, *P.-W. Huang, Y.-C. Kao, S.-Y. Cheng, T.-T. Su*, Lam Research Corporation

Dummy Poly Removal (DPR) is one of the critical processes of hi-K metal gate formation of gate last integration scheme of semiconductor wafer fabrication. A typical DPR process flow includes plasma etching a wafer to open hardmask and to remove dummy poly, then wet etch the wafer with Tetra-Methyl Ammonium Hydroxide (TMAH) to remove any residue that is remained inside the dummy gate trench.

Amorphous silicon is commonly used as the dummy poly materials. A plasma composed of Cl2, HBr, NF3, or combination of above is used to dry etch the dummy poly; however, poly residue defect is observed after DPR process flow. Experimental data indicates that after plasma etch, a Si-O layer is formed on the surface of amorphous silicon which suppress the dummy poly removal capability of the subsequent wet etch. Therefore, dummy poly material is left behind and forms the poly residue defects.

If extended plasma is used to remove the poly residue, the barrier layer (TiN) will be etched and thus damage the hi-K.

To resolve the poly residue defect issue, a post etch treatment (PET) is added after dummy poly is etched by plasma. The purpose of PET is three-folded: it converts the Si-O layer to a layer of which wet etch rate is significantly improved; PET activates the residual F, Cl or Br inside the gate trench and enhance the poly removal; PET has high selectivity to the barrier layer (TiN) and thus TiN film is preserved. The result is no poly residue defects and no hi-K damage.

11:00am **PS-MoM9 Sidewall Roughness Characterization of an Advanced Spacer Patterning Process**, ***Emmanuel Dupuy***, *M. Fouchier, E. Pargon,* CNRS-LTM, France, *J. Pradelles,* CEA-Léti, France, *H. Grampeix,* CEA-LETI, France, *P. Pimenta-Barros, S. Barnola,* CEA, LETI, France, *O. Joubert*, LTM - CEA/LETI, France

Line width roughness (LWR) or line edge roughness (LER) is considered today by the microelectronic industry as a critical factor limiting CMOS transistors downscaling. According to the international technology roadmap for semiconductors, LWR and LER values must be controlled below 2 nm for the next sub-20 nm nodes, which remain a technological challenge for all nanopatterning options and metrology tools. Understanding and minimizing LER at this nanometer scale thus requires an accurate and insightful characterization of the sidewall roughness.

Among advanced nanopatterning solutions, spacer patterning has emerged as a reliable and competitive technique to fabricate fine patterns down to 10 nm. This technique consists in depositing a spacer material on each side of a core (mandrel) defined by lithography and then removing the core to halve the pitch. One critical aspect of this approach is the control of the LER since the spacer patterns are asymmetric from their formation. The right and left sides of the spacer are not obtained by the same technological step and could lead to different LER values on the left and right sidewalls. This behaviour could be problematic if this asymmetry is transferred to the final pattern.

In this work, we propose to characterize and evaluate finely the LWR/LER evolution after each technological step involved in a resist-core spacer patterning process targeting a half-pitch of 20 nm and 10 nm. In this particular case, spacers are directly deposited on the side of the resist. Advantages are less processing steps, a simplified stack and a reduced production cost. A method based on a power spectral density (PSD) analysis is used take into account the noise level of CDSEM images in the LWR/LER estimation of these fine patterns. A full description of the sidewall roughness including its spatial frequency distribution is obtained at each step with an estimation of noise-free parameters such as roughness amplitude (3Ǫ), correlation length (ξ), and roughness exponent (α)." For the 20 nm node, LWR and LER values are drastically reduced to 2.5nm and 2.2nm respectively. The correlation length is found to range from 8 to 22 nm and the roughness exponent from 0.4 to 0.9 for the final silicon lines. Results for the 10 nm node will be discussed in view of evaluating and optimizing process performances.

11:20am **PS-MoM10 Improving Pattern Fidelity for Selective Etch Processes**, ***Nathan Marchack***, *S.U. Engelmann, E.A. Joseph, R.L. Bruce, H. Miyazoe, E.M. Sikorski,* IBM T.J. Watson Research Center, *T. Suzuki, M. Nakamura,* ZEON Chemicals L.P., *A. Itou, H. Matsumoto*, Zeon Corporation

As critical dimensions and pitch sizes of integrated circuit technologies continue to decrease, the challenges associated with maintaining pattern transfer fidelity become especially difficult to surmount. LER/LWR, CD variation, iso/dense feature loading and deformation of the organic soft masks are commonly observed phenomena. Other issues include extensive plasma damage or mask retention for post-lithography solutions.[1]

Our team recently introduced a new etch gas which is able to etch nitride by selective deposition of a fluorocarbon layer[2], analogous to the well established oxide etch mechanism commonly used in manufacturing.[3] Selective deposition was achieved by redesigning the FC etch gas, where reaction with a nitride substrate layer reduces the FC film thickness compared to silicon or oxide substrates. Owing to the complex, distinct nature of the reaction pathways offered by this new plasma chemistry, optimizing the etch performance involves tuning plasma parameters that have not been traditionally investigated. We have evaluated the influence of substrate and showerhead temperatures, gas admixture chemistry and plasma pulsing on the performance of this etch gas for hard mark patterning applications.

By tuning the chemical admixture of the plasma, 50nm pitch patterning of an 80nm thick nitride hard mask layer using a 65nm carbon mask was achieved with greatly reduced LER/LWR (~2.3/2/7) and minimal iso/dense feature loading compared to a traditional CF_4/CHF_3 mixture (LER/LWR ~5/8). The use of plasma pulsing, as well as lowering the lid temperature, was found to increase the carbon mask retention while maintaining reduced LER/LWR. The effect of lid temperature was shown to be related to gas dissociation, which was observed through full spectrum OES spectra collected. The improved mask retention under these conditions allowed for LER/LWR to be reduced even further by reducing the aspect ratio of the structures.

1. S. Engelmann et al., Proc. SPIE 8328-9

2. S. Engelmann et al., AVS 58th Int. Symp. & Exhibit. (2011)

3. M. Schaepkens et al., J. Vac. Sci. Technol. A 17, 26 (1999)

Authors Index

Bold page numbers indicate the presenter