Plasma Science and Technology
Room: 308 - Session PS-MoA

Advanced FEOL/Gate Etching

Moderator: Eric A. Joseph, IBM Research Division, T.J. Watson Research Center

2:00pm **PS-MoA1 Breaking Through Limits in Semiconductor Technology**, ***Chang-Jin Kang***, Samsung Electronics, Republic of Korea **INVITED**

[Abstract]

Our current IT industry, which possesses a strong demand of personal mobile devices, is accelerating towards smart devices with the convergence of new technologies.

Under these circumstances, the development of semiconductors with high speed, high density, low power and high reliability are crucial. Scaling down of devices and to ensuring cost-effective technologies are the two most important tasks the semiconductor industry is facing.

To find proper solutions for the development of future devices and to overcome the limitations of current technologies, mid and long-term projections of future silicon technology as well as DRAM, NAND and Logic technology trends will be covered.

2:40pm **PS-MoA3 Mechanism of Silicon Damage during N_2/H_2 Block Etching for FinFET CMOS**, ***Tamotsu Morimoto***, Tokyo Electron Limited, Japan, *H. Ohtake*, Tokyo Electron America, Inc., *T. Wanifuchi*, Tokyo Electron Miyagi Limited, Japan

In this study, we found that the degradation of a silicon active area during N_2/H_2 block etching strongly depends on ion energy and flux because ions generate significant damage on the silicon surface as compared with the damage to the active area due to hydrogen radicals.

Plasma-induced damage on Si substrates has become a serious concern in CMOS fabrication processes. In addition, the appearance of Fin-FETs have made it necessary for plasma etching processes to use masks made by the organic film opening process and block etching in order to implant the P- or N-type regions. In this study, part of the fin structure was exposed to plasma during organic block etching. It was found that the source and drain regions of the fin area were damaged. However, the impact of the generated damaged layer on the electrical properties has not been clarified, especially junction leakage of the source and drain. In this paper, effect of etching using N_2/H_2 gas combination on p–n junction leakage current at reverse bias was investigated. Parameters of the N_2/H_2 plasma like flow rate, etching time, peak-to-peak voltage of the RF bias (V_{pp}), and the micro wave power (MW) were varied. Si substrate with a p–n junction was exposed to the N_2/H_2 plasma, followed by nickel silicidation to enable electrical characterization.

Junction leakage current increased by increasing V_{pp} and reducing MW for fixed etching times and was independent of the hydrogen ratio in the N_2/H_2 gas. This indicates that ion has a stronger influence on Si damage than H_2 radicals. With etching depth kept fixed, a high hydrogen ratio showed less damage because etching rate was higher. In addition, we obtained smaller damage for higher V_{pp} at constant MW because etching time was shorter owing to the high etching rate. Accordingly, we can infer that ion energy and cumulative ion flux have a significant impact on the degradation of the p–n junction. From the transmission electron microscopy analysis, the damaged layer, which degraded Si crystallinity, became thicker by increasing the exposure time of the Si substrate to the N_2/H_2 plasma. Most probably, the damaged layer has a lot of defect sites which act as trap sites beside the junction, which in turn causes the p–n junction leakage current to increase.

We found that the ratio of ion/radical in the plasma should be lower to reduce the damage of silicon active area by N_2/H_2 block etching. High etching rate and low V_{pp}, which correspond to high hydrogen ratio and low RF bias, is the best combination for low-damage organic block etching.

3:40pm **PS-MoA6 Plasma Etch in the Era of Atomic Scale Fidelity**, ***Vahid Vahedi***, *J. Marks*, Lam Research Corp **INVITED**

The ultimate goal of IC manufacturing is to produce the structures that are conceived and modeled by design engineers in the real world with high fidelity. We choose the term “fidelity” deliberately to express that what is needed in the end is the highest possible degree to which a material structure matches the design intent. It includes but is not limited to statistical criteria such as accuracy and precision.

Plasma etch plays a key role in obtaining structural fidelity in all three dimensions. Precision is obtained by means of wafer- to- wafer, chamber-to- chamber and tool- to- tool matching. Accuracy on the other hand requires control of proximity and 3D effects such as critical dimension (CD) loading, profile loading, aspect ratio dependent etching (ARDE), and selectivity.

As we approach devices with a half pitch of 10 nm and below, atomic scale fidelity is required because the device dimensions and their allowed tolerances are of the same order of magnitude as the inter-atomic distances in the crystal lattice. This type of performance can be obtained when the material is removed layer by layer. The etch process is comprised of single unit steps which repeat in cycles. Each step uses the simplest possible chemistry to surgically target specific reactions at the wafer surface such as activation, removal, and passivation. We call this layer- by- layer etch with atomic fidelity Atomic Layer Etchatomic layer etch1.

In this presentation, we introduce the framework of high productivity, production- worthy ALE atomic layer etch and the implications for hardware and process development. Results for both dielectric and conductor etch obtained with Lam’s Research’ latest etch products will be presented.

References:

1. Kanarik, et al., Solid State Technology, (2013) 14-17.

4:20pm **PS-MoA8 Challenges of 3D NAND Staircase Patterning Process**, ***Hui Zhou***, *S. Srinivasan, J. Choi, A. Khan, L. Yu, Z. Yao, A. Agarwal, S. Rauf*, Applied Materials Inc.

NAND memory microfabrication is at the transition point to vertical structures. A variety of 3D NAND device designs have been reported, such as bit cost scalable (BiCS) and terabit cell array transistor (TCAT). Despite the difference in the structures and operational mechanisms of 3D NAND devices, the microfabrication processes share a common first step, the formation of the landing pads for the control gate via contacts. The “staircase” of pad landings is realized by alternating film etching and resist trimming. To ensure high yield, the registration for the vias must be ensured by the insitu staircase patterning process with CD uniformity being the most critical figure of merit for desired yield. CD uniformity is most sensitive to the resist trimming process and is controlled by plasma distribution and electrostatic chuck temperatures. Local CD non-uniformity may originate from microloading effect or asymmetry impact, and the approaches to improve the local CD uniformity focus on mitigating loading and reducing the asymmetry with process and hardware development, that are also supported by quantitative modeling results. Early versions of the staircase patterning process resulted in low throughput due to multiple resist trimming steps. High throughput is required to reduce the cost of fabrication. Power, flow, and pressure are effective knobs in improving the resist trimming rate. Reducing the gas transition time and using continuous plasma between different gas has also proven effective for further improving throughput. Challenges and progress for 3D NAND staircase patterning process will be discussed, and innovative hardware and process solutions will also be presented.

4:40pm **PS-MoA9 Impact of the Addition of $SiCl_4$ in a $CH_3F/O_2/He$ Chemistry for the Nitride Spacer Etching of FDSOI 14 nm Technology**, *C. Arvet, S. Lagrasta*, ***Maxime Garcia Barros***, STMicroelectronics, France, *S. Barnola, N. Posseme*, CEA, LETI, MINATEC Campus, France, *F. Leverd*, STMicroelectronics, France

Today, the choice of chemistry for nitride spacer etching is a CH3F/O2/He based chemistry. But such chemistry leads to 10A and 15A silicon and silicon germanium consumption, respectively. Furthermore the remaining carbon at the silicon or silicon germanium surface can lead to a poor silicon surface quality which does not allow the film regrowth. The optimization of this process is not enough reliable in order to be used in production for the FDSOI 14 nm technologies.

In this context, we investigated the impact of SiCL4 addition to CH3F/O2/He/CH4 chemistry.

Ellipsometry measurements performed on blanket silicon nitride and silicon germanium film allow us to investigate two essential points for the FDSOI 14 nm technologies:

-The resist consumption

-The opportunity to obtain an infinite selectivity of silicon nitride to silicon germanium.

Complementary XPS and FTIR analyses have been performed for a better understanding of the etch mechanisms and will be presented.

These results have been confirmed on patterned structures. TEM analyses have shown no silicon germanium recess with no foot formation after silicon nitride spacer etching and wet cleaning. Finally, the compatibility of this new etch chemistry on epitaxial growth quality will also be presented.

5:00pm **PS-MoA10 Hydrofluorocarbon Gases for Selective, Low-Damage, Silicon Nitride Etching**, ***James Royer***, *R. Gupta, V. Pallem*, American Air Liquide

Maintaining Moore's law has introduced increasingly stringent process requirements for front-end device technologies. These requirements create considerable technical challenges for silicon nitride gate spacer etching. Etch processes must remove thin silicon nitride layers while maintaining stringent physical constraints and chemical integrity of the underlying substrate. Therefore, the etch gases must be tailored with appropriate functionality for selective silicon nitride etching. This study presents hydrofluorocarbon (HFC) etch gases which demonstrate selective etching of silicon nitride with respect to silicon oxide, and poly-silicon. Using a RIE plasma etch tool, the performance of each molecule is studied on blanket wafers and analyzed using spectroscopic ellipsometry, x-ray photoelectron spectroscopy (XPS), and scanning electron microscopy (SEM). Etch rates and selectivities for each HFC are evaluated over a range of O_2 flow to determine the desirable process windows. Select HFCs have large process windows with infinite silicon nitride to poly-silicon selectivity due to fluorocarbon deposition on the poly-silicon. The fluorocarbon deposition layer on poly-silicon inhibits undesired silicon-carbide or silicon-oxide formation. XPS surface analysis and depth profiling shows a reduction in carbon and oxygen incorporation in poly-silicon compared to similar processes using the industry standard molecule, fluoromethane.

5:20pm **PS-MoA11 Alternative Process for Thin Layer Etching: Application to Nitride Spacer Stopping on Silicon Germanium**, ***Nicolas Posseme***, *G. Santini, O. Pollet, C. Arvet, S. Barnola*, CEA-LETI, France

Today, minimizing the so-called silicon germanium (or silicon) recess during nitride spacer etching is extremely difficult to achieve but mandatory since it directly impacts the device performances. Despite of etch chemistry or tool improvement, this silicon germanium recess is only limited.

In this context, we proposed an alternative etching process to overcome these issues and meet the highly complex requirements imposed by device fabrication processes. This new etching process is based on two steps. In a first step, the film is modified in volume by a H_2 plasma performed in a conventional etch tool (ICP or RIE) followed in a second step by a selective removal of the modified layer with respect to the non-modified material.

In this study, we will present this alternative process for nitride spacer etching stopping on silicon germanium for FDSOI devices. It will be demonstrated that the silicon nitride film modification can be adjusted by playing on plasma parameters. XPS and infrared spectroscopy analyses have been performed on blanket silicon nitride film to understand the silicon nitride film modification induced by H_2 plasma . These mechanisms of the silicon nitride film damage will be discussed.

In the meantime, different approaches (dry or wet) to remove the modified silicon nitride film without non-modified nitride or silicon germanium films consumption have also been investigated. The advantages and the drawbacks of these approaches will be presented.

Starting from the best process conditions (modification and removal steps), TEM analyses performed on patterned structures have revealed that the silicon germanium recess is less than 5A for a wide range of nitride film over etch (from 30 to 120%) with no foot formation compared to more than 15A recess and 20 A foot formation using the best current etching processes (CH_3F/O_2/He chemistries targeting 50% over etch).

Finally, the compatibility of this new nitride spacer etching process on SiGe epitaxial growth quality will also be presented. It will be shown, that the clean surface obtained after the modified nitride film removal leads to a perfect epitaxial growth for different silicon nitride over etch from 30 to 120%.

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