Electronic Materials and Processing
Room: 314 - Session EM2-WeM

High-K Dielectrics from Non-Classical Channels
Moderator: Christopher Hinkle, University of Texas at Dallas

8:00am **EM2-WeM1 The Influence of Surface Preparation pre-Atomic Layer Deposition of Al_2O_3 on GaN Metal Oxide Semiconductor Capacitors**, ***Dmitry Zhernokletov***, Stanford University

High-κ gate dielectrics have been proposed as a means of producing high performance field effect devices with low gate leakage on GaN-based substrates for low static power consumption, improved transconductance, and higher output power capabilities [1-3]. However, because the surface of GaN may contain defects such as dangling bonds and contaminants [4], understanding the effect of varying surface preparation prior to atomic layer deposition (ALD) of the high-κ gate dielectrics on GaN is of great importance for the advancement of field effect devices. Surface defects and contaminants such as carbon and oxygen may have detrimental effects on optical quality and device performance of GaN based devices. Several methods to improve GaN surface and interface quality have been proposed [4-8]. They include surface cleaning procedures using aqueous $(NH_4)_2S$, and acid/base treatments such as HCl, HF, NaOH and NH_4OH.

We present a detailed study on the influence of surface preparations pre-atomic layer deposition of Al_2O_3 on GaN metal oxide semiconductor capacitors. The electrical, chemical, and luminescence characteristics of MOS structures prepared on both chemically treated and as-received GaN substrates are reported. Aqueous NH_4OH cleaning shows promise for providing an enhanced starting surface for atomic layer deposition of Al_2O_3 layers on GaN.

[1] P.D. Ye et al., Appl. Phys. Lett. 86, 063501 (2005).

[2] O.I. Saadat et al., IEEE Electron. Dev. Lett. 30 1254-1256 (2010).

[3] D.J. Meyer et al., Solid-State Electron.5 1098 (2010).

[4] R.D. Long et al., Materials. 5, 1297-1335 (2012).

[5] Diale et al., Appl.Surf.Sci. 246, 279–289 (2005).

[6] Lee et al., J. Electrochem. Soc. 147, 3087–3090 (2000).

[7] Hattori et al. Surf. Sci. 2010, 604, 1247–1253.

[8] Y. Koyama et al.,Solid State Electron.43,1483–1488 (1999).

8:20am **EM2-WeM2 Low Voltage Nonlinearity Metal-Insulator-Insulator-Metal (MIIM) Capacitors using Plasma Enhanced Atomic Layer Deposition of SiO_2 and Al_2O_3**, ***Dustin Austin***, Oregon State University, *D. Allman, D. Price, S. Hose,* On Semiconductor, *J.F. Conley*, Oregon State University

Back end of line (BEOL) metal-insulator-metal (MIM) capacitors reduce the need for discrete off-board components and have become a core passive device in integrated circuits. Applications include analog-to-digital converters, analog noise filters, DC voltage decoupling, and electrostatic discharge (ESD) protection. To enable continued scaling, capacitance density must be increased, either by introducing higher dielectric constant (κ) materials or by reducing the insulator film thickness. However decreasing insulator film thicknesses increases both leakage current density and voltage nonlinearity (characterized by the quadratic voltage coefficient of capacitance or αVCC). In addition high-κ materials typically have a large positive αVCC. Although a promising route to simultaneously meeting these competing requirements is to use a nanolaminate of insulators, which allows for combining of layers with complementary properties. Previous work has demonstrated nanolaminate MIIM devices with high capacitance density, low leakage current density, and low αVCC using PECVD SiO_2 or uncommon materials. [1–3]

In this work, MIIM capacitors using bilayers of Al_2O_3 and SiO_2 were deposited sequentially using plasma enhanced atomic layer deposition (PEALD). PEALD allows for low deposition temperatures, precise thickness control, and conformal coverage over high aspect ratio structures. Al_2O_3 and SiO_2 are attractive due to their common usage in IC fabrication, large metal-insulator barrier heights, and high dielectric breakdown strength. In addition SiO_2 is one of the few materials that exhibits a negative αVCC. Spectroscopic ellipsometry was used to characterize the growth rate and nucleation delay on TaN and Si substrates. The dielectric constants of Al_2O_3 and SiO_2 were found to be 4.6 and 8.7, respectively. αVCC values were plotted as a function of thickness and fit with a power law. Appropriate layer thicknesses were chosen to offset the negative αVCC of SiO_2 with the positive αVCC of Al_2O_3 in order to minimize the effective αVCC for a given capacitance density. The initial results for 8 nm Al_2O_3 / 3.5 nm SiO_2 MIIM devices show capacitance density of 5.4 fF/μm^2, 2 nA/cm^2 leakage at 1V, and αVCC of 70 ppm/V^2, simultaneously meeting the ITRS 2014 requirements for capacitance density (> 5 fF/μm^2), leakage current density (< 10 nA/cm^2 at 1V), and voltage nonlinearity (< 100 ppm/V^2). Current work is underway to optimize this nanolaminate to meet the ITRS 2017 requirements.

[1] S. Van Huylenbroeck et al, Electron Device Lett. IEEE 23, 191 (2002).

[2] S.J. Kim et al, Electron Device Lett. IEEE 25, 538 (2004).

[3] T.H. Phung et al, Electrochem. Soc. 158, H1289 (2011).

8:40am **EM2-WeM3 Metal-Insulator Transitions, Resistive Switches and Oxide Electronics**, ***Shriram Ramanathan***, Harvard University **INVITED**

There is growing interest in the exploring complex oxide semiconductors as functional elements in solid state devices. this is in part created by the inevitable limits to use of traditional semiconductors in highly scaled devices and also expanding interest in integrating multiple functionalities at the chip-level. Dielectrics with engineered defects and correlated oxides could be potentially interesting in this regard as switchable, adaptive materials for interconnects, logic and memory. There are a number of fundamental issues from the materials and interface aspects that remain poorly understood. For example, how can we develop a quantitative understanding of the electrical aspects of the high-k / correlated oxide interface where in almost all cases, such phase change materials show drastic frequency dependent properties? How can we design gate stacks to modulate carrier density approaching that of metallic state in such oxides? In this presentation, I will address these problems, with emphasis on studies conducted in our laboratory on rutile (e.g. VO2) and perovskite (e.g. SmNiO3) structured oxide thin films that undergo insulator-metal transitions.

9:20am **EM2-WeM5 Complex Oxide Devices**, ***Suman Datta***, Penn State University **INVITED**

Strongly correlated electronic phases encountered in complex oxides exhibit collective carrier dynamics that if properly harnessed can enable novel functionalities and perhaps even new computation paradigms. In this talk, we will present our recent understanding of electronically triggered charge oscillations in a prototypical metal insulator transition (MIT) system, vanadium dioxide. We show that the key to such oscillatory behavior lies in the ability to stabilize a spontaneously reversible phase transition in the complex oxide devices using a negative feedback mechanism. We also explore the synchronization dynamics of such oscillators via experiment and simulation, and investigate its potential for coupled oscillator based non-Boolean associative computing.

11:00am **EM2-WeM10 Ferroelectric Devices**, ***Alexander Demkov***, The University of Texas at Austin **INVITED**

Novel methods of deposition developed over the past decade or so, enabled fabrication of thin films of ferroelectric materials, such as $BaTiO_3$ (BTO), of very high crystal quality. This has resulted in renewed interest in ferroelectric field effect transistors and in addition, led to new device architectures, such as negative capacitance devices. Thanks to very high Pockels coefficient, thin films of BTO may find applications in Si nano-photonics.

In this talk I will describe our recent efforts on integration of BTO (and other ferroic oxides) on semiconductors using a $SrTiO_3$ (STO) buffer. More specifically, I will describe integration of $BaTiO_3$ on Si (001) and Ge (001) using molecular beam epitaxy (MBE) and atomic layer deposition (ALD). We employ first principles modeling to both guide the crystal growth and analyze the characterization data. By modeling core level spectroscopy and comparing it with the x-ray photoemission data we are able to identify the Zintl growth template for STO on Si and Ge. Comparing theoretical spectral functions with the angle resolved photoemission spectra (ARPES), provides us with a better understanding of the $SrTiO_3$ buffer surface. Using this strategy we stabilized ferroelectric state with out-of-plane polarization in $BaTiO_3$ (BTO) grown on Si with an STO buffer. And we demonstrate both out-of-plane in-plane polarized BTO growth on Ge (001). Annular dark field microscopy is used to elucidate the atomic structure of the semiconductor/oxide interface that is used in subsequent first principles calculations of the band alignment at the interface. We use a combination of polarization force and microwave impedance microscopies to investigate the ferroelectric response and field effect in our structures.

This work is done in collaboration with Patrick Ponath, Kurt Fredrickson, Agham Posadas, John Ekerdt, David Smith, Martin Frank, Vijay Narayanan, Catherine Dubourdieu, Sergei Kalinin and Keji Lai. It is supported by the Air Force Office of Scientific Research under grant FA9550-12-10494, Office of Naval Research (ONR) under grant N000 14-10-1-0489, National Science Foundation under grant DMR- 1207342, and Texas Advanced Computing Center.

11:40am **EM2-WeM12 Enhanced Performance Metal/Insulator/Insulator/Metal (MIIM) Tunnel Diodes**

*N. Alimardani, **JohnF. Conley, Jr.***, Oregon State University

Thin film metal-insulator-metal (MIM) tunnel devices are gaining interest for applications such as hot electron transistors, diodes for optical rectenna based IR energy harvesting, IR detectors, large area macroelectronics, and selector diodes to avoid the sneak leakage in RRAM crossbar arrays. For many of these applications, figures of merit include high asymmetry and strong nonlinearity of current vs. voltage (I-V) behavior at low turn on voltages (V_{ON}). The common strategy to achieving rectification in MIM devices relies on Fowler-Nordheim tunneling (FNT) conduction in conjunction with the use of dissimilar work function metal electrodes to produce an asymmetric, polarity dependent electron tunneling barrier. The properties of single layer MIM diodes are dominated by the choice of insulator. Performance is limited by the workfuction difference that can be achieved between the electrodes as well as the metal-insulator band offsets. Wide bandgap oxides are limited by high V_{ON}. Narrow bandgap dielectrics such as Ta_2O_5 and Nb_2O_5 are attractive because the small barrier heights allow for low turn-on voltages. However, because conduction in these materials is based on emission rather than tunneling, they may not be suitable for high speed rectification. Recently, we showed that a nanolaminate pair of insulators (Al_2O_3/HfO_2) can be used to form MIIM diodes with enhanced performance over single layer MIM diodes and demonstrated that observed enhancements in low voltage asymmetry are due to "step tunneling," a situation in which an electron may tunnel through only the larger bandgap insulator instead of both.[1]

In this work, we show that MIIM diodes may require only one of the insulators to be dominated by tunneling and thus allow use of narrow band gap insulators for tunnel devices. Atomic layer deposition (ALD) was used to deposit nanolaminate insulators on smooth amorphous metal bottom electrodes. We demonstrate that Ta_2O_5, a narrow bandgap dielectric dominated by thermal emission, may be combined with Al_2O_3, a wide bandgap dielectric dominated by tunneling, to achieve high asymmetry, low V_{ON} MIIM diodes whose overall performance is dominated by tunneling. The performance of a variety of other bilayer MIIM diodes (HfO_2/Ta_2O_5, ZrO_2/Ta_2O_5, Al_2O_3/ZrO_2, and HfO_2/ZrO_2) will be discussed as well. These results advance the understanding needed to engineer thin film tunnel devices for microelectronics applications.

1. N. Alimardani and J.F. Conley, Jr., Appl. Phys. Lett. 102, 143501 (2013).

12:00pm **EM2-WeM13 Assessment of Barrier Heights between ZrCuAlNi Amorphous Metal and SiO_2, Al_2O_3, and HfO_2 using Internal Photoemission Spectroscopy**

Tyler Klarr, Oregon State University*, L. Wei, N.V. Nguyen, O.A. Kirillov,* National Institute of Standards and Technology (NIST)*, J. McGlone, J. Wager, J.F. Conley*, Oregon State University

As scaling of Si based devices approaches fundamental limits, thin film metal-insulator-metal (MIM) tunnel diodes are attracting interest due to their potential for high speed operation. Because operation of these devices is based on tunneling, electrode / interfacial roughness is critical. Recently, we showed that combining ultra-smooth bottom electrodes with insulators deposited via atomic layer deposition (ALD) enabled reproducible fabrication of MIM diodes with stable I-V behavior.[1] Key performance parameters of MIM diodes include high I-V asymmetry and low turn-on voltage. The standard way to achieve asymmetry relies on the use of non-equivalent workfunction metal electrodes to induce a built-in field that creates polarity dependent electron tunneling barrier.[2] Assessment of metal-insulator barrier heights is therefore critical for predicting diode performance.

In this work, we report the first use of internal photoemission spectroscopy (IPE) to measure barrier heights between an amorphous ZrCuAlNi (ZCAN) metal bottom electrode and several high-k dielectrics. MIM stacks were fabricated on Si substrates capped with 100nm of thermally grown SiO_2 and a 150nm thick ZCAN amorphous metal bottom electrode deposited via DC magnetron sputtering. Al_2O_3 and HfO_2 were deposited via thermal ALD at 250ºC using H_2O and TMA or TEMA-Hf, respectively. SiO_2 was deposited using plasma-enhanced ALD (PEALD) at 200ºC using O_2 and bis-diethylaminosilane (BDEAS). For IPE measurements, semitransparent top electrodes were formed by electron beam evaporation of Al (0.04mm^2) and patterned by a multistep photolithography process. In IPE, the conduction band offset between two materials is characterized by measuring the additional current created by photo-excitation of carriers under an applied bias (V_{app}). Devices were tested in a custom built IPE system in which incident photon energy (E_{ph}) from a broadband 150W xenon lamp source was swept from 1.5 to 5eV while the increase in current (photoemission yield) was monitored. The V_{app} polarity was such that photoemission occurs at the ZCAN/insulator interface. The photoemission yield$^{1/2}$ was plotted vs. E_{ph} to determine the spectral threshold at each V_{app}. Finally, a Schottky plot of spectral threshold vs. $V_{app}^{1/2}$ was used to estimate the zero field barrier heights from the y-axis intercept. Initial analysis indicates barriers of 3.4, 3.2, and 2.7 eV for SiO_2, Al_2O_3, and HfO_2, respectively. Additional dielectrics and metals are under investigation. IPE results will be compared to electrical methods of barrier extraction.

1. N. Alimardani et al, JVSTA 30, 01A113 (2012).

2. J.G. Simmons, JAP 34, 2581 (1963); JAP 34, 1793 (1963).

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