Thursday Morning, November 13, 2014

Electronic Materials and Processing
Room: 314 - Session EM2-ThM

High-K Dielectrics for ReRAM and RAM
Moderator: John Conley, Oregon State University

8:00am **EM2-ThM1 Challenges and Materials Solutions for Memristive Devices (ReRAM)**, ***Jianhua(Joshua) Yang***, HP Labs **INVITED**

Memristive devices (also known as RRAM when used for memory) are electrical resistance switches that can retain a state of internal resistance based on the history of applied voltage or current, which can be used to store and process information for computing systems beyond CMOS technologies. These devices have shown great scalability, switching speed, non-volatility, analogue resistance change, non-destructive reading, 3D stack-ability, CMOS compatibility and manufacturability. However, there are still a number of challenges facing memristive devices for real applications, including device variability and isolation in a crossbar array. This talk will discuss and address these challenges from the materials perspective.

8:40am **EM2-ThM3 Physical Mechanisms and Scaling of the Resistive Memory (ReRAM)**, ***Daniele Ielmini***, *S. Balatti, S. Ambrogio*, Politecnico di Milano, Italy **INVITED**

The resistive memory (ReRAM) is attracting strong interest from the industry and academia for its low-power, high-speed and nonvolatile behavior. ReRAM properties are compatible with many of the requirements of storage (e.g., the solid state drive, or SSD) and memory (e.g., SRAM or DRAM), thus ReRAM may potentially revolutionize computing architectures in the future. While ReRAM has been recently introduced in the ITRS, the industrial programs for device development, volume production and commercial exploitation are still challenged by the lack of understanding about device physics, reliability and scaling.

This work will discuss the recent progress on the understanding of ReRAM physics. First, a numerical model for ReRAM switching will be described, highlighting the primary role of defect migration driven by Joule heating and electric field. The model will be tested under several conditions of voltage and currents, showing the model capability to identify new operation modes for self-select ReRAM and enhanced multilevel operation. Finally, the scaling issues will be addressed, explaining the device variability data with the aid of a Monte Carlo model for discrete defect migration. The fundamental tradeoff between power reduction and device reliability will be finally discussed.

9:20am **EM2-ThM5 Variability of Metal Oxide Based RRAM: Challenges and Opportunities**, ***An Chen***, GLOBALFOUNDRIES **INVITED**

Recently, metal-oxide based resistive-RAM (RRAM) has emerged as a promising nonvolatile memory (NVM) candidate. However, it is also recognized that the stochastic RRAM switching mechanisms inevitability introduce large variability in device parameters, which impose severe challenges for memory applications especially in high-density arrays. RRAM variability can be attributed to the microscopic variation of dimension and/or composition of the filamentary conductive paths during the switching process. Variability in switching voltage/current reduces safe operation margin and resistance variation degrades sensing margin. Cell-to-cell and cycle-to-cycle variability has different origins and needs to be differentiated in RRAM characterization. Resistance variability measured by □/μ (deviation/mean) has to be controlled within target ranges determined by device and array specifications. Mechanism and typical characteristics of RRAM variability will be reviewed in this presentation. Although variability is undesirable for memory arrays, security applications embrace truly random variations. Pervasive and ubiquitous computing requires robust light-weight security technologies at low cost. Physical unclonable functions (PUF) exploit physical randomness and variability as security primitives. RRAM variability may be utilized for PUF implementation, which may achieve much smaller footprint than existing PUF solutions. Feasibility of PUF designs based on RRAM variability will be analyzed based on measured device properties

11:00am **EM2-ThM10 High-K Development for DRAM, NAND, and ReRAM Applications**, ***Nirmal Ramaswamy***, Micron Technology **INVITED**

DRAM, NAND and ReRAM utilize high-K oxides to enable high performance devices . High-K oxides are deployed as capacitor dielectrics in DRAM, blocking dielectrics in NAND and solid state electrolytes to enable ion motion in ReRAM. The material and electrical properties required to enable these different technologies are widely different. Several critical parameters such as dielectric constant, band offset, trap density, modulus, crystallinity and texture have to be simultaneously optimized for each technology. This talk highlights the performance requirements of advanced memory devices and the high-K materials engineering required to enable these devices.

11:40am **EM2-ThM12 Resistive Switching Characteristics and Mechanism in Oxide Conductive-Bridge RAM**, ***Ming Liu***, *Q. Liu, H.B. Lv, S.B. Long*, Chinese Academy of Sciences, China **INVITED**

Conductive bridging RAM (CBRAM) has been intensively investigated for the application of next generatin nonvolatile memories due to its excellent scalability and superior switching performances [1-2]. Generally, the device forms by an ion-conducting insulator sandwiched between an oxidezable electrode (i.e. Cu or Ag) and an inert electrode (i. e. Pt or W). The resistance switching is based on the the formation and annihilation of nanoscale metallic conductive filament (CF) in the ion-conducting insultator under the external power. This kind of filament utilizes composition of metal ions transferring from the oxidizable electrode to the inert electrode due to cation redox reaction [2]. Deep understanding of the CF dynamic growth mechanism and development of controllable CF growth method will help to guide the design of CBRAM devices with desirable properties. Using binary oxide, such as ZrO and HfO , we successfully obtained some CBRAM devices with excellent resistive switching performances [3-4]. Based on the variable temperature testing and the advanced SEM and TEM analysising, some fundamental issues related to the resistive switching effect, including the morphologies, chemical compositions and dynamic growth/dissulution of CFs were directly addressed in various CBRAM systems [5]. In addtion, using “electrical engineering”, we demonstrated that the CF growth process can be controlled by modulating distribution electric field inside ion-conducting insulator, which greatly improving the uniformity of the CBRAM device [6].

Reference:

[1]. R. Waser, M. Aono, Nat. Mater. 2007, 6, 833.

[2]. J. J. Yang, D. B. Strukov, D. R. Stewart, Nat. Nanotechnol. 2013, 8, 13.

[3]. Q. Liu, S. Long, W. Wang, S. Tanachutiwat, Y. Li, Q. Wang, M. Zhang, Z. Huo, J. Chen, M. Liu, IEEE Electron Device Lett. 2010, 31, 1299.

[4]. Y. Li, H. Lv, Q. Liu, S. Long, M. Wang, H. Xie, K. Zhang, Z. Huo, M. Liu, Nanoscale 2013, 5, 4785.

[5]. Q. Liu, J. Sun, H. Lv, S. Long, K. Yin, N. Wan, Y. Li, L. Sun, M. Liu, Adv. Mater. 2012, 24, 1844.

[6]. Q. Liu, S. long, H. Lv, W. Wang, J. Niu, Z. Huo, J. Chen, M. Liu, ACS Nano 2010, 4, 6162.

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