Wednesday Morning, November 12, 2014

Electronic Materials and Processing
Room: 311 - Session EM1-WeM

Materials and Devices for High Power Electronics (8:20-11:00 am)/Two Dimensional Electronic Materials & Devices (11:00 am - 12:20 pm)
Moderator: Andrew Antonelli, Lam Research, Rachael Myers-Ward, U.S. Naval Research Laboratory

8:00am **EM1-WeM1 Commercialization of High Voltage GaN HEMT.**, *P. Parikh, **Rakesh Lal***, Transphorm Inc. **INVITED**

With its proven ability to reduce size (improved form factor) and save energy (improved efficiency) Gallium Nitride (GaN) is now no longer a nice to have, it is a must have for power conversion. In applications have emerged ranging from sub 100 watt ultra-compact high frequency adapters to multi kilowatt highly efficient PV Inverters, GaN makes it possible to do what Silicon cannot. High voltage GaN on Silicon HEMT switches are now a reality, following successful completion of JEDEC qualification as well as establishment of a high voltage lifetime of 100M hours. A large area (6inch) Silicon substrate, epitaxial processes that promise to leverage the commercial success of the well established GaN LED & lighting products and the ability to manufacture in existing high volume Silicon foundries makes GaN commercially attractive. Successful companies need to deliver high quality product with a deep understanding of how the GaN switch is best utilized in applications. We will discuss the commercialization of the GaN power HEMT by Transphorm - enabled by execution on the above fronts, a strong intellectual property across the full value chain and a strong team with deep rooted experience in GaN technology and business. Ultimately GaN is expected to significantly reduce conversion losses endemic in all areas of electricity conversion, ranging from power supplies to PV inverters to motion control to electric vehicles, enabling consumers, utilities and Governments to contribute towards a more energy efficient world.

8:40am **EM1-WeM3 Progress and Future Challenges in SiC Material for High-Voltage Power Devices**, ***Tsunenobu Kimoto***, Kyoto University, Japan **INVITED**

Silicon carbide (SiC) is an emerging wide bandgap semiconductor, by which high-voltage, low-loss power devices can be realized owing to its superior properties. SiC unipolar devices such as Schottky barrier diodes and MOSFETs will replace Si unipolar/bipolar devices in the blocking-voltage range from 600 V to about 6500 V. Regarding SiC power MOSFETs, the authors developed vertical trench MOSFETs in collaboration with ROHM. The trench MOSFETs with cell miniaturization exhibited extremely low on-resistances of 0.79 mΩcm^2 and 1.4 mΩcm^2 for 630 V and 1260 V devices, respectively, with normally-off characteristics [1]. After reliability tests, all-SiC power modules (1200 V – 180 A) are now commercial products.

For ultrahigh-voltage applications above 6500 V, SiC bipolar devices such as PiN diodes and IGBTs are promising. Major technological challenges include fast epitaxy of thick (> 100 µm) and high-purity epilayers, stress control, reduction of basal-plane dislocations and stacking faults, enhancement and control of carrier lifetimes. The authors succeeded in fast epitaxial growth of 100-200 µm-thick SiC at a growth rate of 40-85 µm/h with a high purity (1×10^{13} cm^{-3}) and reduced density of basal-plane dislocations. Through elimination of the $Z_{1/2}$ center, a lifetime killer in SiC, via thermal oxidation, the authors obtained about 200 µm-thick, $Z_{1/2}$-free n-type SiC epilayers, where the bulk lifetime reaches 30 µs or even longer [2]. The carrier lifetimes can be controlled by low-energy electron irradiation, which can preferentially generate the $Z_{1/2}$ center (carbon vacancy) in SiC.

Ultrahigh-voltage PiN diodes were fabricated by using lightly-doped (2-3×10^{14} cm^{-3}) SiC epilayers with different thicknesses (50-260 µm). The breakdown voltage was scaled with increasing the epilayer thickness, as simulated. The maximum breakdown voltage experimentally obtained exceeded 27 kV, which is the highest blocking voltage among any solid state devices. The differential on-resistance was remarkably reduced by enhancement of carrier lifetimes, being 2 mΩcm^2 and 10 mΩcm^2 for 13 kV and 27 kV devices, respectively. A SiC bipolar junction transistor with a blocking voltage over 21 kV and current gain over 60 was also demonstrated [3].

This work was supported by the Funding Program for World-Leading Innovative R&D on Science and Technology (FIRST Program) and a Grant-in-Aid for Scientific Research from JSPS. The authors acknowledge Dr. T. Nakamura with ROHM for the MOSFET collaboration.

[1] T. Nakamura et al., Tech. Digest. 2011 IEDM, 26.5.1.

[2] S. Ichikawa et al., Appl. Phys. Exp., **5**, 101301 (2012).

[3] H. Miyake et al., IEEE Electron Device Lett., **33**, 1598 (2012).

9:20am **EM1-WeM5 4H-SiC Epilayers Grown on 2° Offcut Substrates**, ***Rachael Myers-Ward**, Z.R. Robinson, V.D. Wheeler, P.B. Klein, N.A. Mahadik, R.E. Stahlbush, C.R. Eddy, Jr., D.K. Gaskill*, Naval Research Laboratory

Silicon carbide is a material of interest for high-voltage, high-power switching device applications. Basal plane dislocations (BPDs) are a major concern for SiC bipolar devices as they source Shockley-type stacking faults in the presence of an electron-hole plasma and reduce minority carrier lifetimes [1]. Many researchers have investigated methods to reduce BPD densities by experimenting with pre-growth treatments [2-4], substrate orientation [5], growth parameters [5, 6] and growth interrupts [7]. This work investigates extended defects, morphology and lifetime in 4H-SiC epilayers grown on substrates offcut 2° toward the [11-20].

Epilayers were grown in a horizontal hot-wall reactor using silane (2% in H_2) and propane. Hydrogen etching was conducted to determine the morphology of the substrate during the ramp to growth temperature; temperatures explored were 1400, 1450 and 1500 °C. Epilayers were grown at various growth rates of 1, 5 and 10 µm/hr and C/Si ratios from 1.0 to 1.55. The influence of doping with ultra-high purity nitrogen was investigated. Ultraviolet photoluminescence (UVPL) imaging was used to identify BPDs in low doped epilayers. Time resolved photoluminescence measurements were performed to determine the minority carrier lifetime of the layers and Raman spectroscopy was used to analyze polytype inclusions. Surface roughness was measured by atomic force microscopy and Nomarski microscopy was also used to characterize morphology.

No step bunching was found when the temperature was raised to 1400 °C in H_2 and cooled down immediately. However, intermittent step bunching formed when the temperature was raised to 1500 °C. When a 15 µm epilayer was introduced, step bunching was observed and the surface roughness was 6.0 nm RMS. For comparison, a standard 4° offcut sample typically has 3.0 nm RMS for a 20 µm epilayer. Using UVPL, it was found that after 4 µm of epi, 90% of the BPDs had converted in the epilayer as compared to 70% in a 4° offcut sample, indicating the conversion is faster in the lower offcut material. Epilayers without any BPDs were observed; however, 3C-SiC inclusions were present as verified by Raman spectroscopy. BPD densities and carrier lifetimes of the epilayers will also be reported.

[1] J.P. Bergman, et al. Mater. Sci. Forum Vol. **353-356**, 299 (2001).

[2] Z. Zhang, et al., Appl. Phys. Lett. **89**, 081910 (2006).

[3] J.J. Sumakeris, et al., Mater. Sci. Forum **527-529**, 529 (2006).

[4] H. Tsuchida, et al., Mater. Sci. Forum **483-485**, 97 (2005).

[5] W. Chen and M.A. Capano J. Appl. Phys. **98**, 114907 (2005).

[6] T. Ohno, et al., J. Cryst. Growth **271**, 1 (2004).

[7] R.E. Stahlbush, et al., Jr., Appl. Phys. Lett. **94**, 041916 (2009).

11:00am **EM1-WeM10 Recent Progress in Graphene and Heterostructure RF Electronics**, ***Jeong-Sun Moon**, H.-C. Seo, K.A. Son, B. Yang, M. Antcliffe, A. Schmitz, D. Le,* HRL Laboratories, LLC, *L.O. Nyakiti, V.D. Wheeler, R.L. Myers-Ward, C.R. Eddy, D.K. Gaskill,* Naval Research Laboratory, *K.-M. Lee, P. Asbeck*, University of California at San Diego **INVITED**

Graphene is a truly 2D electronic material with a very high intrinsic saturation velocity (V_{sat}) of ~5×10^7 cm/sec, which has great potential for high-speed RF applications. In addition, graphene offers unique properties, such as high mobility, excellent scalability, symmetry in electron or hole channel, its ability to be integrated into any substrate, and its potential compatibility with CMOS.

The material quality and fabrication process for graphene have improved with sheet resistance of ~200 ohm/sq, ohmic contact resistance of ~0.03 W×mm, the lowest on-state resistance of 0.13 W×mm, and the highest saturated source-drain current of ~3 A/mm at Vds = 1 V. Recently, graphene FETs (GFETs) demonstrated zero-bias resistive FET mixer operation up to 20 GHz [1] with 10 times improvement in the mixer quality factor (IIP3/total power) over state-of-the-art (SOA) resistive FET mixers; these GFETs also demonstrated zero-bias in power detectors and radiometers (up to 220 GHz) [2] with linear-in-dB dynamic range with >20 dB improvement over SOA FETs. Graphene heterostructure-based FETs have been developed as enhancement-mode FETs with an Ion/Ioff ratio of >10^5 and excellent pinch-off and I-V saturation [3]. Graphene varactors

have been demonstrated on glass substrates, expanding graphene's potential to be integrated with arbitrary substrates, and potentially enabling active and tunable antenna surfaces beyond wafer-scale.

In this talk, we present recent progress in graphene material, GFETs, graphene heterostructure FETs, circuit applications for mixers, radiometers, detectors, varactors, and progress toward integrating graphene with active antennas. Continuous development of this emerging material would potentially enable RF systems on nonconventional surfaces.

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[1] J.S. Moon et al., IEEE Electron Device Letters., vol 34, p465, 2013; J. S. Moon and D. Kurt Gaskill, IEEE Trans. Microwave Theory and Tech., vol. 52, pp 1014-1024, 2011.

[2] J. S. Moon et al., IEEE Electron Device Letters., vol 33, p1357, 2012.

[3] J.S. Moon et al., IEEE Electron Device Letters., vol 34, p1190, 2013

11:40am **EM1-WeM12 High-Field and Thermal Transport in 2D Atomic Layer Devices**, ***Eric Pop**, C.D. English,* Stanford University*, V.E. Dorgan, A. Behnam,* University of Illinois at Urbana-Champaign*, Z. Li,* Stanford University, University of Illinois, Urbana-Champaign*, S. Islam*, University of Illinois at Urbana-Champaign **INVITED**

Two-dimensional (2D) materials like graphene and transition metal dichalcogenides (TMDs) are uniquely suited for nanoscale field-effect transistors (FET) due to sub-nm channel thickness and lack of dangling surface bonds. Thus, unlike three-dimensional (3D) materials such as Si, FETs based on 2D materials would be more resilient to short-channel effects and would suffer less mobility degradation from carrier-surface scattering. Nevertheless, most existing studies of 2D materials have focused on large devices and low-field transport. By contrast, highly scaled 2D-FETs will require very good understanding of electric transport at high fields and thermal transport as relevant for large scale device integration.

In this talk we will describe our recent progress in optimizing transport at 2D-3D material contacts, examining high-field transport, FET scaling and thermal measurements at sub-100 nm device dimensions. For instance, we have recently uncovered transport physics at TMD and 2D graphene contacts with metal electrodes, including the roles of metal deposition conditions during fabrication and that of thermoelectric (Peltier) effects during transistor operation [1,2]. We will also describe our understanding of high-field transport in MoS2 and graphene, including the importance of self-heating effects on various substrates such as SiO2, BN and HfO2 [3,4]. Finally, we will describe our thermal measurements in suspended graphene [5] and in graphene devices with dimensions comparable to the electron and phonon mean free paths (~100 nm) [6]; the former yield the intrinsic behavior of this material, while the latter show quasi-ballistic thermal transport near room temperature, as well as significant phonon-edge scattering in narrow devices. The results are of importance for both electronic and thermal applications of 2D materials.

References

[1] K.L. Grosse, M.-H. Bae, F. Lian, E. Pop, W.P. King, Nature Nano. 6, 287 (2011)

[2] C.D. English, V.E. Dorgan, G. Shine, K. Saraswat, E. Pop, IEEE Device Research Conf. (2014)

[3] M.-H. Bae, S. Islam, V.E. Dorgan, E. Pop, ACS Nano 5, 7936 (2011)

[4] S. Islam, Z. Li, V.E. Dorgan, M.-H. Bae, E. Pop, IEEE Electron Device Lett. 34, 166 (2013)

[5] V.E. Dorgan, A. Behnam, H. Conley, K. Bolotin, E. Pop, Nano Lett., 13, 4581 (2013).

[6] M.-H. Bae, Z. Li, Z. Aksamija, P.N. Martin, F. Xiong, Z.-Y. Ong, I. Knezevic, E. Pop, Nature Comm. 4, 1734 (2013)

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