Thursday Afternoon, November 13, 2014

Electronic Materials and Processing
Room: 311 - Session EM1-ThA

Materials for Quantum Computation
Moderator: Sang M. Han, University of New Mexico

2:20pm **EM1-ThA1 Mos Quantum Bits for Adiabatic and Non-Adiabatic Quantum Computing**, *Malcom Carroll*, Sandia National Laboratories **INVITED**
This talk will describe silicon nanostructures that confine electrons at the SiO2/Si interface and produce quantum dot behavior. These structures combined with single ion implantation provide a platform for silicon quantum bits. Application of these structures towards circuit model and ground state quantum computing approaches will be discussed. We acknowledge the research funding support provided by the laboratory directed research and development (LDRD) program at Sandia National Laboratories. Sandia National Labs is a multi-program laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the United States Department of Energy's National Nuclear Security Administration under contract DE-AC04-94AL85000.

3:00pm **EM1-ThA3 ^{28}Si Enriched *In Situ* to 99.9998 % for Quantum Computing Devices**, *Kevin Dwyer*, University of Maryland, College Park, *J. Pomeroy, D. Simons*, National Institute of Standards and Technology (NIST)
We are enriching *in situ* and depositing epitaxial thin films of ^{28}Si in support of quantum computing devices. Highly enriched ^{28}Si is a critical material for quantum computing as removal of ^{29}Si spins provides a non-interacting "semiconductor vacuum" medium for qubits such as ^{31}P donors which have electron and nuclear coherence (T_2) times of seconds and minutes respectively even up to room temperature. ^{31}P donors can also be addressed optically due to hyperfine transitions not normally resolvable in natural Si. Starting with natural abundance silane, we have used mass filtered ion beam deposition to produce ^{28}Si films enriched to > 99.9998 % with a residual ^{29}Si isotope fraction < 1 ppm (40 times less than previously reported ^{28}Si sufficient for optical addressing). Using our ion beam system we have grown crystalline ^{28}Si films and are pursuing characterization of their structural properties using *in situ* reflection high energy electron diffraction (RHEED), *in situ* scanning tunneling microscopy (STM), and transmission electron microscopy (TEM). Secondary ion mass spectrometry (SIMS) is used to determine enrichment of crystalline ^{28}Si films. As we move away from silane towards a solid sputtering source, enrichment may be improved even further and the use of additional materials such as Ge can become possible. Numerous experimental systems can take advantage of ^{28}Si as a medium for qubits including STM based hydrogen lithography devices, single donors coupled to single electron transistors, and quantum wells. We have demonstrated the ability to produce isotope heterostructures with applications including fully enriched ^{28}Si/^{28}Si^{74}Ge quantum wells. The importance of ^{28}Si to quantum information systems and the scarcity of such material make clear the critical need for an alternate source of enriched silicon such as the one we demonstrate.

3:20pm **EM1-ThA4 Computational Analysis of Interdiffusion in Silicon-Germanium Alloy Films Subject to Patterned Stress Fields**, *Daniel Kaiser*, University of Pennsylvania, *S. Ghosh, S.M. Han*, University of New Mexico, *T.R. Sinno*, University of Pennsylvania
In this talk we present a multi-element computational approach for quantitatively describing atomic interdiffusion within a random-alloy SiGe wafer subject to a patterned stress field imposed by an indenter array applied to its surface. The model, and the associated parametric investigations we carry out, are motivated by a recently-proposed approach for forming ordered arrays of heteroepitaxial Ge quantum dots (QD) on semiconductor substrates in a scalable and robust manner. In this approach, patterned compositional redistribution of Si and Ge atoms is driven by an applied stress field under thermal annealing. The resulting compositional heterogeneity is shown to induce an internal stress field in the SiGe substrate wafer that persists after the indenter array is removed, thereby effectively "transferring" the stress pattern of the indenter into the substrate. The transferred stress pattern, which we study in detail as a function of several parameters including indenter geometry and thermal annealing schedule, is then used to drive patterning in a subsequent Ge deposition step.

The interdiffusion model is based on a combination of lattice kinetic Monte Carlo (LKMC) and static energy minimization. The LKMC simulation is propagated using rates for atomic diffusion that depend explicitly on local values of stress, composition, and temperature. The dependence of atomic diffusion on composition is regressed to experimental data while the stress dependence is described using the theory of activation volumes [1]. The stress field is updated quasi-statically using a separate energy minimization routine with forces computed based on a Tersoff interatomic potential for the Si-Ge system [2]. The atomic stresses and identities are then smoothed to generate continuous fields that are used as input into the LKMC simulation.

Using our model, we establish that atomic redistribution is feasible for reasonable indenter forces and annealing times and temperatures. We compute the corresponding internal stresses in the compositionally patterned film for several different annealing conditions and show that these stresses are likely to be large enough to influence subsequent Ge quantum dot nucleation and growth. We also compare our results to recent experimental measurements.

References:

[1] M. J. Aziz, Applied Physics Letters 70, 2810 (1997).

[2] J. Tersoff, Physical Review B 39, 5566 (1989).

4:00pm **EM1-ThA6 Scanning Capacitance Microscopy of Atomically-Precise Donor Devices in Si**, *Shashank Misra*, *E. Bussmann, M. Rudolph, S.M. Carr, G. Subramania, G. Ten Eyck, J. Dominguez, M.P. Lilly, M. Carroll*, Sandia National Laboratories
Recently, a scanning tunneling microscopy (STM) technique to fabricate atomically-precise dopant-based nanoelectronics in Si has been developed. Phosphorus donors are placed via an atomic-precision template formed by STM H-depassivation lithography, then capped with epi-Si and lastly metal contacts are made to the buried donor layer using conventional microfabrication. New challenges are introduced with this approach that center around difficulties to locate and characterize the pattern of buried donors. In this talk, we show that scanning capacitance microscopy (SCM) can image these buried donor nanostructures with sub-100-nm tip-limited resolution. The technique is used to successfully locate and characterize buried donor nanostructures relative to surface alignment marks. This approach relaxes alignment requirements for the STM lithography step and can offer improved alignment of subsequent metallization steps. The SCM technique is also used to nondestructively image the shape of the electronic carrier distribution and characterize the relative doping levels. This work, performed in part at the Center for Integrated Nanotechnologies, a U.S. DOE Office of Basic Energy Sciences user facility, was supported by Sandia's Lab Directed Research and Development Program. Sandia is a multi-program lab operated by Sandia Corp, a Lockheed-Martin Company, for U. S. DOE under Contract DE-AC04-94AL85000.

4:20pm **EM1-ThA7 SiGe on sSOI: Nanoscale Engineering of Structures and Devices on Surfaces**, *Esmeralda Yitamben*, *E. Bussmann*, Sandia National Laboratories, *R. Butera*, Laboratory for Physical Sciences, *S. Misra, M. Rudolph, S.M. Carr, M. Carroll*, Sandia National Laboratories
The relentless increase in both density and speed that has characterized microelectronics, and now nanoelectronics, will require a new paradigm to continue beyond current technologies. One proposed such paradigm shift demands the ultimate control over the number and position of dopants in a device, which includes quantum information processing and variety of semiconductor device materials and architectures aimed at solving end-of-Moore's law issues.

Such a work requires the development of a tool for the design of atomically precise devices on silicon and other surfaces, in hope of studying the effect of local interactions between atomic-scale structures, their microscopic behavior, and how quantum mechanical effects might influence nano-device behavior in very small structures. Demonstrations of remarkable 2D nanostructures down to single atom devices are reported here thanks to the development of scanning tunneling microscopy (STM) as an imaging and patterning tool. These include atomic-scale depassivation of a hydrogen terminated surface with an STM, toward the incorporation of dopants in silicon, and SiGe growth on strained silicon on insulator (sSOI). sSOI has been shown to be relatively insensitive to thermal relaxation and thereby provides a starting material that satisfies the requirements of both enabling high temperature surface preparation steps combined with providing a strained layer that can be capped with relaxed SiGe forming a high quality interface for gate tunable channel formation. In this talk we will present, STM and other characterization results on cleaning, hydrogen lithography, dopant incorporation and SiGe growth on sSOI.

Acknowledgments: This work was performed, in part, at the Center for Integrated Nanotechnologies, a U.S. DOE, Office of Basic Energy Sciences user facility. The work was supported by the Sandia National Laboratories

4:40pm EM1-ThA8 Creating a Responsive SiGe Substrate to Form 2D Array of Ge Quantum Dots Using Stress-induced Near-surface Compositional Redistribution, *S. Ghosh*, University of New Mexico, *D. Kaiser, T.R. Sinno,* University of Pennsylvania, *Sang M. Han*, University of New Mexico

A well-defined array of Ge quantum structures possesses unique electronic properties for a variety of applications, including quantum-computers and infrared photodetectors. Herein, we use simulation to predict and experiment to demonstrate the compositional redistribution of Si and Ge in the near-surface region of $Si_{0.8}Ge_{0.2}$ substrates by applying a spatially structured compressive stress to the substrate and thermally annealing the substrate under stress. The primary advantage of the proposed approach is that a single, reusable template is used to induce the compositional variation for multiple substrates. The compositional redistribution of Ge is predicted under purely elastic deformation, using a lattice kinetic Monte-Carlo simulation that accounts for the influence of composition, temperature, and stress on the diffusion kinetics of Ge in SiGe alloy. Atomistic stress field in a SiGe slab is computed using the Tersoff empirical potential and static relaxation. This compositional variation in turn can be used to selectively grow a 2D array of Ge quantum dots upon Ge exposure. To complement the computational prediction, the compressive stress is applied by pressing a 2D array of Si pillars against the $Si_{0.8}Ge_{0.2}$ substrate. Hertz contact model is used to calculate the compressive stress applied to the $Si_{0.8}Ge_{0.2}$ substrate under the Si nanopillars. We observe that the magnitude of compressive stress and annealing temperature determine the nature of deformation (elastic or plastic) in the $Si_{0.8}Ge_{0.2}$ substrate. Corresponding energy dispersive x-ray spectroscopy (EDS) shows that the compositional redistribution of Si and Ge in the near-surface region of $Si_{0.8}Ge_{0.2}$ substrates results from elastic deformation within a thermal annealing temperature range of 950 to 1000 °C and an applied stress range of 15 to 18 GPa. Based on nano-probe EDS, the elastically deformed compressed region shows near-complete Ge depletion and Si enrichment in atomic concentration. However, the temperature and stress exceeding the aforementioned ranges result in plastic deformation with no compositional variation. The plastic deformation depth is ~30 nm according to scanning transmission electron microscope images. We attribute the plastic deformation to (1) the localized pressure applied to the substrate under the contact area, (2) the near-surface substrate stiffness at substrate temperature, and (3) the tensile biaxial stress under the compressed region due to different thermal expansion rates of Si vs. $Si_{0.8}Ge_{0.2}$.

5:00pm EM1-ThA9 DFTMD Modeling of Atomic Scale Structure Requirements for amorphous Sub 0.5 EOT Gate Oxides, *T. Kent, T. Kaufman-Osborn, M. Edmonds, S.W. Park, J.H. Park, I.J. Kwak, E.A. Chagarov,* University of California, San Diego, *P. Choudhury,* New Mexico Institute of Mining and Technology, *R. Droopad,* Texas State University, *Andrew C. Kummel*, University of California, San Diego

For EOT scaling below 0.5 nm on FinFETs, it is necessary to nucleate the ALD in 99% of the unit cells on multiple crystallographic faces to obviate the requirement that the oxide overgrow non-reactive unit cells. (1) DFTMD calculations of high-k/InGaAs stacks annealed at 700K show that oxide bonding to each InGaAs surface atom in each cell is critical to avoid dangling bonds creating conduction band edge states; this requires high ALD nucleation by a metal precursor density follow by oxidation of any metal-metal bonds formed during nucleation.. For III-V semiconductors, experimental STM and STS studies show the in-situ exposure of just a few hundred Langmuirs of atomic H readily removes both group V and group III oxides from 001 and 110 surfaces allowing high nucleation density of metal ALD precursors. Concurrent MOSCAP studies show demonstrate sub 0.5 nm EOT gate oxides with low defect densities on InGaAs after in-situ cleaning and high nucleation density ALD. (2) DFTMD studies of the a-Al_2O_3/SiGe(001) stack show that the SiGe(001) interface with Si termination (a-Al_2O_3/Si-SiGe(001)) has a superior electronic structure to the interface with Ge termination (a-Al_2O_3/Ge-SiGe(001). Silicon termination of SiGe should also be highly favorable for forming gas passivation of dangling bonds. For SiGe(001) a novel technique has been develop to produce surface which will mimic the good passivation properties of Si(001) by terminating the surface in a monolayer of Si-OH which will react with nearly any metal ALD precursor. (3) While group IV and III-V semiconductors can be nucleated by covalent bonds, 2D semiconductors require a different approached. DFTMD simulation studies show the metal coordination complexes can readily chemisorb on 2D semiconductor via non-bonding interaction and they can covalent bond multiple TMA molecules consistent with a submolecular nucleation density. A technique has been develop for functionalize 2D semiconductors with a

phthalocyanine, and it has been demonstrated it can nucleate insulation sub 1nm gate oxide growth.

5:20pm EM1-ThA10 Crystalline $SrHfO_3$ Grown Directly on Ge (001) by Atomic Layer Deposition as a Gate Oxide for High-Mobility Ge-based Transistors, *Martin McDaniel, T.Q. Ngo, A.B. Posadas, C. Hu, S.N. Chopra, E.T. Yu, A.A. Demkov, J.G. Ekerdt*, The University of Texas at Austin

Crystalline strontium hafnate, $SrHfO_3$ (SHO), is an ideal candidate to study as a suitable high-*k* gate dielectric on Ge. SHO ($a \sim 4.069$ Å) has a reasonable lattice match to the Ge (001) surface ($a/\sqrt2 \sim 3.992$ Å), yielding a ~1.9% compressive strain in the epitaxial film. SHO shows a high permittivity (k~20) with appropriate band alignment (~1 eV offset) to Ge. In addition, the crystalline nature of the SHO film is expected to drastically reduce the interface trap density at the oxide-Ge interface. We will report our recent results on the growth, characterization, and electrical performance, of epitaxial SHO films and heterostructures for next-generation high-*k* dielectrics on Ge.

In our recent publication, we reported on the direct growth of crystalline strontium titanate, $SrTiO_3$ (STO), on Ge via atomic layer deposition.[1] Electrical measurements of a 15-nm thick undoped STO film show a large dielectric constant (k~90), but high leakage current (~10 A/cm^2 at +1 eV). In the present work, the unfavorable conduction band offset (and high leakage current) of STO on Ge is circumvented by growing the Hf-based perovskite, SHO. For the growth of SHO, we employ the commercially available strontium bis(triisopropylcyclopentadienyl) and hafnium formamidinate precursors. After thermal deoxidation, the Ge substrate is transferred *in vacuo* to the deposition chamber where a thin film of SHO (2-4 nm) is deposited by ALD at 225 °C. Following post-deposition annealing at 700 °C, the perovskite film becomes crystalline with epitaxial registry to the underlying Ge (001) substrate. *In situ* x-ray photoelectron spectroscopy confirms stoichiometric to Sr-rich films with no GeO_x formation or carbon impurities.

Ex situ x-ray diffraction confirms the perovskite structure and orientation of the SHO film. Thicker SHO films (above 2 nm) appear to show a relaxed lattice constant, indicating relaxation of the epitaxial film above the critical thickness. The electrical performance of several SHO films and heterostructures will be presented. In general, the leakage current is reduced by several orders of magnitude for the SHO films versus STO on Ge. The current work demonstrates the promise for crystalline oxides grown by ALD on Ge for advanced semiconductor devices, including high-mobility Ge-based transistors.

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[1] M. D. McDaniel *et al.*, "A Chemical Route to Monolithic Integration of Crystalline Oxides on Semiconductors," accepted to *Adv. Mater. Interfaces* (2014), doi: 10.1002/admi.201400081.

5:40pm EM1-ThA11 The Influence of Carbon Incorporation into Gd_2O_3 High-k Gate Dielectric on the Electronic Behavior of the MOS Stack, *Pini Shekhter*, Technion Israel Institute of Technology, Israel, *A.R. Chaudhuri*, Leibniz University, Germany, *A. Laha,* Indian Institute of Technology Bombay, India, *H.J. Osten,* Leibniz University, Germany, *M. Eizenberg*, Technion Israel Institute of Technology, Israel

High k dielectric materials receive great attention in recent years due to the downscaling of metal-oxide-semiconductor (MOS) devices leading to the need in replacing the traditionally used SiO_2 gate oxide. Rare earth oxides are leading candidates as high-k dielectrics. Introduction of different elements into the bulk of such oxides can drastically alter the behavior of the MOS stack.

Here we present the results of incorporation of carbon into the bulk of Gd_2O_3 on the electrical properties of the Pt/Gd_2O_3:C/Si stack. Crystalline layers of stoichiometric Gd_2O_3 were MBE deposited together with elemental C on Si (100) substrates. Four samples with different concentration of elemental C were prepared: 0%, 0.10%, 0.67%C and 1.89%. MOS capacitors were prepared by in-vacuo (in the MBE tool) evaporating Pt through a shadow mask.

Capacitance voltage (C-V) measurements revealed an increase in the flatband voltage (V_{fb}) for the carbon rich sample. While the three samples with the lower carbon content all showed V_{fb} voltages of -0.1 ÷ +0.2 V, the sample with 1.89% carbon presented a significant increase to 2.25 V.

X ray diffraction (XRD) revealed that all the layers hold the same structure and that no orientation differences are present in the layers, ruling out the option of structural differences leading to such a change in V_{fb}. Time of flight secondary ion mass spectroscopy (ToF-SIMS) depth profiles revealed an uneven concentration profile for the carbon in the 0.67% and 1.89% samples. For both samples, the same concentration was found in the bulk of the layer, indicating the existence of a certain solubility limit that had been exceeded. This led to some segregation for the 0.67% sample to the inner

interface while substantial segregation was observed in the 1.89% sample to the inner interface and some to the outer surface. Transmission electron microscope (TEM) micrographs show a thin amorphous interface layer that is formed between the Gd_2O_3 and Si that most likely plays a role in the capturing of the segregating carbon atoms.

We propose that the carbon segregation causes a modification of V_{fb} which is an important property of the MOS stack. By using carbon incorporation it might be possible to develop an effective method for controlling V_{fb} without changing the process or materials for any of the MOS gate components.

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