Electronic Materials and Processing
Room: 314 - Session EM-TuM

Advanced Interconnects and Materials
Moderator: Sean King, Intel Corporation, Andrew Antonelli, Lam Research

8:00am **EM-TuM1 Cu/ULK ULSI On-Chip Wiring Technologies, and Related Devices**, ***Daniel Edelstein***, IBM **INVITED**

We are familiar with microelectronics "scaling" (reducing dimensions) of integrated circuits, so they get denser and cheaper (Moore 's Law), and faster (Dennard's Law), in turn increasing the computational power of IC chips. Perhaps less appreciated is that scaling has always gone against the performance and reliability of the multilevel on-chip wiring, commonly termed "Back End of the (Manufacturing) Line", or BEOL, needed to connect these circuits. This invited talk focuses on forefront efforts in materials and nano-scale engineering to combat BEOL scaling and extendibility problems.

Our work has begun on the 7 nm CMOS node, with our 11th generation Cu BEOL. The smallest wires are ~17 nm wide, (< $1/10^{th}$ the lithographic wavelength!), and represent ~1/25x scaling from the 1^{st} Cu generation. As we migrate to these dimensions, significant innovations in patterning and metallization have been required to preserve defect-free fabrication and electromigration reliability. In order to reduce parasitic wiring capacitance, with its signal delay and power loading, our insulator dielectric constants have migrated from 4.1 to 2.4. But in turn, these materials get more fragile, both electrically and mechanically, requiring significant learning in interface and material mechanics, plus dielectric reliability physics.

Concurrently, system-level performance and cost scaling push more diverse functions onto the chip, and into the wiring levels. Recent innovations add new devices to the finer wiring levels, as well as "reverse-scaled" (larger) wiring levels allow us to collapse more diverse packaging functions onto the chip. Examples of what we fabricate will be presented, with some of their integration-specific issues and solutions. These include ultrathick Cu for data bandwidths, high-Q and magnetic inductors for RF and voltage converters, MEMs switches for antenna diversity, through-Si vias for 3D integration, and magnetic and phase-change non-volatile memory devices (MRAM and PCM).

8:40am **EM-TuM3 Selectivity Characterization and Enhancement of Metal-Organic Chemical Vapor Deposited (MOCVD) Selective Cobalt Cap for Advanced Back End of Line**, ***Jeff Shu***, *Z. Sun, Y.B. Lee, J. Palazzo, Z. Bayindir, M. Hossain, S. Choi, J. Rullan, H. Liu*, GLOBALFOUNDRIES U.S. Inc.

The continuous shrink of Cu interconnect feature size leads to higher current densities, which lower electromigration lifetimes. The interface between post chemical mechanical polishing (CMP) Cu and dielectric cap has been identified as a key diffusion path for copper atoms, and the adhesion of the interface is critical to electromigration performance [1]. Alternate metallization schemes for copper interconnect using selective CVD Co capping are considered for 22nm technology and below from integration point of view, metal-organic deposition selectivity is the key for leakage and reliability. During the selective CVD Co deposition, both Cu and porous ultra low k dielectric surface are exposed to the metal-organic precursor, insufficient selectivity will increase metal line to line leakage, degrade metal shorts and time-dependent dielectric breakdown (TDDB) performance. In this paper, we focus on selectivity characterization and enhancement of MOCVD selective Co cap process. Selectivity of different precursors are thoroughly evaluated and compared. Lower reaction rate of the carbon based organic group of the Co precursor and the reducing agent was demonstrated to benefit selectivity. Different ultra low k films with various porosity also play a big role in selectivity. Key tuning knobs for the process window have been defined as process pressure and temperature. The quantity of final Co deposition on porous ultra low k surface has been measured by both X-ray fluorescence (XRF) and Total Reflection X-ray Fluorescence (TXRF), which will subsequently be applied to the definition of selectivity, with comparison to the amount on polished Cu surface. XRF measurement shows some disadvantage due to weak signal to noise ratio while TXRF measurement results are more reliable. X-ray photoelectron spectroscopy (XPS) is used to profile the oxygen penetration into pristine film and the self-limited cobalt oxide thickness has been measured at 15A to 25A, which can be modulated by vacuum break between Co cap and dielectric cap, and by surface pre-clean process before dielectric cap deposition.

[1] J. R. Lloyd , M.W. Lane, E. G. Liniger, "Relationship between interfacial adhesion and electromigration in Cu metallization" 2002 IEEE International Integrated ReliabilityWorkshop Final Report, p.32 - 35 (2002)

9:00am **EM-TuM4 Precise Control of the Residual Stress Levels in Polycrystalline Thin Films for Advanced Interconnects and N/MEMS Applications**, ***Hang Yu***, *C.V. Thompson*, Massachusetts Institute of Technology

Precise control of residual stress in polycrystalline thin films, which remains a central but difficult task in advanced interconnects and N/MEMS applications, requires synergistic manipulation of multiple processing parameters. Our recent work has demonstrated that stress evolution during film growth is controlled by a series of kinetic processes that include adatom-ledge interactions on the surfaces of individual grains, adatom interactions with grain boundaries, and grain growth during film thickening. By synergistically controlling the growth conditions and therefore controlling these kinetic processes, residual stress levels in polycrystalline films can be tailored for optimal performance for specific given applications. In particular, we find that the composition and partial pressure of residual gases in the deposition chamber have a profound effect on the stress evolution behavior. As a consequence, understanding and control of these effects allow tuning of the residual stress of a film. As an example, we demonstrate the use of low levels of oxygen impurities to produce zero stress Ni films.

9:20am **EM-TuM5 CVD Mn-based Barrier for Advanced Copper Interconnect Technology: Integration Study**, ***Nicolas Jourdan***, IMEC, Belgium

To prevent copper diffusion in a circuit, commonly a PVD-TaN/Ta liner is formed on the dielectric surface as a diffusion barrier prior to Cu metallization. The integrity of the PVD-TaN/Ta barrier is expected to reach its limit at a trench dimension below 20nm width. As a result, alternatives must be found for further technology scaling. In recent years, Mn-based barriers have received great consideration as a thin self-formed MnSixOy diffusion barrier can be formed at the surface of the insulator without significant impact on the dielectric constant whilst preserving the total trench volume for Cu filling. Initially, such a "zero-thickness barrier'' has been made using a PVD-CuMn seed layer, from which Mn atoms diffuse after a thermal anneal towards the surface of the insulator to form the diffusion barrier. However, because of the use of PVD, limited scalability of this option is expected. Therefore, CVD of Mn-based chemistries has been developed to enable the formation of a thin and conformal barrier [1, 2]. Such a layer has already been integrated in 2ML test vehicles (half pitch ranging from 40nm to 100nm) using a conventional scheme consisting of a PVD-Cu seed followed by Cu electroplating (ECD) and CMP. The authors reported significant RC reduction and comparable Time Dependent Dielectric Breakdown (TDDB) performance with respect to conventional PVD-TaN/Ta barrier [3]. However, integration of a thin Mn-based barrier faces a big challenge due to Mn dissolution taking place in the chemistries used in ECD and CMP operations. The impact of such a phenomenon is even more dramatic in narrow trenches used for advanced technology nodes due to the scaled PVD-Cu seed, which is no longer able to sufficiently protect Mn from dissolution.

In this work, we focus on the optimization of CVD Mn-based barrier in order to make it integration friendly. Furthermore, we will report on physical properties of such a barrier.

[1] N. Jourdan et al.: Electrochemical and Solid-State Letters 15 (5) (2012) H176-H178.

[2] Roy G. Gordon et al.: Proc. Advanced Metallization Conference, p. 1 (2008).

[3] Y. K. Siew et al., Proc. IEEE IITC 2013, p. 1.

9:40am **EM-TuM6 Cryogenic Etching vs P4 Approaches: Paths towards Ultra-low Damage Integration of Mesoporous Oxide Dielectric Materials**, ***Jean-Francois de Marneffe***, IMEC, Belgium, *L. Zhang, M.H. Heyne, M. Krishtab,* IMEC, KU Leuven, Belgium, *A. Goodyear, M. Cooke,* Oxford Instruments Plasma Technologies, *N. Heylen, I. Ciofi, L.G. Wen, C.J. Wilson,* IMEC, Belgium, *V. Rutigliani,* University Bari, Italy, *S. Decoster,* IMEC, Belgium, *T. Savage,* SBA Materials, Inc., *K. Matsunaga, K. Nafus,* Tokyo Electron Kyushu Limited, Japan, *J. Boemmels, Z. Tokei, M. Baklanov*, IMEC, Belgium

In recent year, two innovative strategies have been proposed to decrease plasma-induced low-k damage: the P4 approach [Frot et al., 2011] and the cryogenic etch approach [Zhang et al., 2013]. The P4 or "pore stuffing" uses an extrinsic sacrificial pore filler, allowing protection during plasma

etching and metallization steps. The cryogenic etch is based on in-situ pore filling by etch byproducts and/or $SiOF_x$ sidewall passivation.

In this work, a PMO spin-on material with pristine k = 2.31 from SBA has been integrated on 300mm wafers. The integration vehicle uses narrow-spacing structures, i.e. 30nm low-k lines at 180nm pitch.

For the cryogenic etch approach, after lithography, the SiC/SOC/SOG hardmask is trimmed and opened using standard etch. Low-k etching is performed by means of a SF_6-based plasma chemistry in an ICP chamber equipped with a liquid-N_2 cooled substrate holder set at a base temperature of -120°C. Careful optimization of etch conditions allows to considerably decrease the loss of Si-CH_3 bonds, keeping an acceptable etch rate, good hardmask selectivity, and reduced bottom roughness. After patterning and subsequent byproduct removal by annealing, a conventional Cu metallization is performed using TaNTa barrier, Cu seed and electroplating. After chemical-mechanical polishing (CMP) and SiC passivation, functional circuits gave integrated dielectric constant of k_{int} = 2.38, i.e. showing a $\Delta k = 0.07$ relative to pristine.

For the pore stuffing approach, PMMA was used as filling material and driven in after low-k deposition. Due to thermal instability of PMMA, a low-temperature Si_3N_4 hardmask was used, as well as low-temperature TaNTa barrier. PMMA was removed after CMP, by means of He-H_2 downstream plasma ashing or thermal decomposition. Functional circuits gave integrated dielectric constants k_{int} = 2.73 (thermal unstuffing) and k_{int} = 3.14 (He-H_2 ashing).

By comparison of both approaches, it is observed that pore stuffing increases interconnect flow complexity, by the addition of stuffing and unstuffing steps which can also damage the low-k material; however post-etch surfaces are smooth and barrier metal penetration is suppressed. The pore stuffing approach could be improved by using more thermally stable polymers and the search for damage-free unstuffing methods. The current cryogenic etch process requires only minor changes into the process flow, however currently it requires a base temperature of -120°C. The cryogenic etch process could be improved by the use of plasma additives enhancing by-products condensation and/or pre-condensation steps. We acknowledge support from the European Union under grant agreement No. 318804 (SNM).

11:00am **EM-TuM10 Reliability of Advanced Interconnects**, ***Carl V. Thompson***, Massachusetts Institute of Technology **INVITED**

As interconnect dimensions have continued to shrink with each new CMOS generation, increased electrical resistivity has had a growing impact on overall circuit performance. This has driven the search for radical changes in interconnect technologies based, for example, on nanomaterials such as carbon nanotubes and graphene. However, with kilometers of interconnect per integrated circuit subject to stringent yield and reliability requirements, viable alternatives to metal-based interconnects have not yet been found. Therefore, for the foreseeable future, further improvements in IC performance and functionality will require evolutionary advances in interconnect materials systems. Recent work on performance enhancement has focused on reduced surface and grain boundary scattering in Cu, and the use of dielectric environments with low dielectric constants. These developments are constrained by the need to maintain high reliability, and sometimes come at the expense of reliability. Also, performance improvements can sometimes be enabled by reliability improvements and changes in design constraints imposed by reliability concerns. Design and layout strategies that lead to improved interconnect reliability and allow relaxation of constraints imposed by reliability concerns will be reviewed. The impact on evolving technologies on electromigration-limited reliability will also be discussed, as will needed changes in reliability assessment methodologies.

11:40am **EM-TuM12 Metal Resistivity Below 10 nm**, ***Daniel Gall***, *P. Zheng, D. Guan,* Rensselaer Polytechnic Institute*, J.S. Chawla,* Intel Corporation*, T. Zhou*, Rensselaer Polytechnic Institute

Electron scattering at surfaces and grain boundaries causes the resistivity of metals to increase with decreasing wire width or film thickness. This effect is quantified using (i) *in situ* transport measurements on single-crystal, atomically smooth Cu(001) layers, (ii) textured Cu(111) layers and patterned Cu wires with independently varying grain size, thickness and line width, (iii) *in situ* grown interfaces including Cu-Ni, Cu-Ta, Cu-MgO, Cu-Ti, Cu-SiO_2 and Cu-oxygen, and (iv) epitaxial layers of various other metals including Ag(001), W(001), Ta(001), Ni(001), and TiN(001). The layers are grown by ultra-high vacuum magnetron sputter deposition on MgO(001) substrates and are found to be atomically smooth single crystals by a combination of x-ray diffraction θ-2θ scans, ω-rocking curves, pole figures, reciprocal space mapping, Rutherford backscattering, x-ray reflection, transmission electron microscopy, and *in-situ* scanning tunneling microscopy.

The measured resistivity is interpreted within the classical models by Fuchs and Sondheimer for surface scattering and Mayadas-Shatzkes for grain boundary scattering. The data is well described by these models. However, fitting of the resistivity vs thickness for metal layers with non-spherical Fermi surfaces provides values for the bulk electron mean free paths that deviates from the expected free-electron values by factors of 5-10, indicating the breakdown of these semiclassical models. In addition, the F-S model also does not correctly predict the temperature dependence, as the measured scattering specularity as well as the product of bulk resistivity times mean free path are temperature dependent.

First-principles density functional (DFT) calculations are employed to develop an understanding of electron transport in metals at reduced length scales: (i) The Fermi surface of the bulk metal is determined and the electronic-structure contribution to the conductivity calculated by integration over the Brillouin zone. This provides, in combination with the known bulk resistivity, values for the bulk electron mean free path of 40, 3.3, and 16 nm for Cu, Ta, and W, respectively. (ii) Application of the Boltzmann transport equation and simultaneous integration over real and reciprocal space of the thin film and Brillouin zone, shows considerable anisotropy effects. For example, electron scattering at a W(100) surface has a two times larger effect on the resistivity than scattering on W(110). (iii) Simulation of transport using the 2D Fermi surfaces of thin films, and (iv) non-equilibrium DFT simulations are used quantitatively determine electron scattering which will be directly mapped on a phenomenological model.

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