Electronic Materials and Processing
Room: 314 - Session EM+2D-TuA

High-k Dielectrics for Advance Semiconductor
Moderator: Andrew C. Kummel, University of California at San Diego

2:20pm **EM+2D-TuA1 Time-resolved XPS of ALD**, ***Rainer Timm***, Lund University, Sweden **INVITED**

Atomic layer deposition (ALD) has been established as the main technique for creating MOS structures based on III-V semiconductors, but still device performance is limited by the quality of the interface towards the high-k oxide layer. X-ray photoemission spectroscopy (XPS) is a well-suited tool for analyzing the structure and chemical composition of such interfaces. However, conventional XPS studies under ultrahigh vacuum conditions can only compare the situation before and after individual half-cycles of the ALD process. Here I will show how ambient-pressure XPS can be used to study surface structure and chemistry live and *in-situ* during the ALD reaction. As an example, we have investigated the deposition of HfO_2 on InAs using TDMA-Hf and water as precursors, revealing several steps within the chemical reaction of InAs exposed to the Hf precursor material, which we interpret as a temperature-dependent adsorption of unreacted precursor molecules preceding the ligand exchange reaction.

3:00pm **EM+2D-TuA3 GaSb Oxide Thermal Stability Studied by Dynamic-XPS**, ***Stephen McDonnell***, *B. Brennan, E. Bursa,* University of Texas at Dallas, *K. Winkler, P. Baumann,* Omicron NanoTechnology, Germany, *R.M. Wallace,* University of Texas at Dallas

GaSb is a III-V material with applications as a potential channel material for p-type metal-oxide-semiconductor field effect transistors,[1] optoelectronics in the infrared region,[2] quantum devices,[3] and tunnel field effect transistors.[4] Prior to application specific processing it is often necessary to remove the GaSb native oxide, which can be quite thick. Such oxides can inhibit subsequent epitaxy and also be a source of traps for devices as a result of defect levels in the energy gap.[5] The thermal desorption of these oxides in ultra high vacuum has been examined in previous works, but is revisited in this study with dynamic-x-ray photoelectron spectroscopy (dynamic-XPS). Dynamic-XPS allows for the collection of core-level spectra in real time (i.e. data acquisition times are < 1 second). Combined with controlled heating, this allows for detailed chemical temperature-dependent chemical analysis to be carried out with temperature resolutions better than 1 Kelvin. The thermal decomposition of the native GaSb oxides is studied using dynamic-XPS. The expected transfer of oxygen from Sb-O to Ga-O before the eventual desorption of all oxides is observed. However an initial reaction resulting in the reduction of Sb_2O_3 along with the concurrent increase in both Ga_2O_3 and Sb_2O_4 is detected in the temperature range of 450-525 K. Using the relative changes in atomic concentrations of the chemical species observed, the initial reaction pathway is proposed.

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3:20pm **EM+2D-TuA4 Combined Wet HF and Dry Atomic H Cleaning of SiGe followed by Passivation of the Clean Surface via H_2O_2(g) Dosing**, ***Sang Wook Park***, *T. Kaufman-Osborn, E.A. Chagarov, A.C. Kummel*, University of California at San Diego

Silicon Germanium (SiGe) is a well-known material for its high mobility and useful applications in strain engineering. Its advantages can be utilized to overcome the challenges when scaling down silicon-based devices. As the interest in introducing new kinds of materials increases, the cleaning and passivation methods also become more significant in order to provide uniform and clean surfaces, which would result in improved electrical properties such as high mobility and low interface trap density (Dit). In this study, combined wet and dry cleaning and passivation of SiGe(100) surface is discussed, using scanning tunneling microscopy (STM), scanning tunneling spectroscopy (STS), and x-ray photoelectron spectroscopy (XPS).

Wet cleaning using 2% hydrofluoric acid (HF) was implemented to strip the native oxide off the SiGe sample but left residual carbon contamination on the surface. Although the oxide layer was removed, additional oxygen adsorbed to the surface during transfer from the HF solution to vacuum chamber. This residual oxygen can be eliminated by keeping the SiGe sample covered in the HF cleaning solution until the sample is introduced to the vacuum chamber or by transferring the sample in an inert environment. Dry in-situ atomic hydrogen cleaning was then implemented to remove the carbon contamination on the surface. A post deposition anneal at 550˚C was used to obtain an atomically clean, flat, and ordered SiGe surface and this was verified using STM. The oxygen and carbon contaminant levels were monitored after each cleaning procedure using a monochromatic XPS. The clean SiGe sample was dosed at room temperature with a saturation dose of H_2O_2(g). STM and XPS measurements indicate that H_2O_2(g) dosing leaves the SiGe surface, which is mostly Ge atoms due to surface segregation, terminated with an ordered monolayer of Ge-OH sites. STS measurements of the Ge-OH sites show the conduction band edge dangling bond states are eliminated due to the passivating Ge–OH bonds, but the Fermi level is pinned near the valence band edge due to the large surface dipole. When the surface is annealed to 310°C, XPS measurements indicate that the –OH species on the surface break bonds with the Ge atom and bond instead to the Si atoms, raising Si atoms towards the surface. XPS also verifies that no oxygen leaves the surface due to the 310°C anneal. Instead, the oxygen remains on the surface in the form on Si-OH or SiO_x species. TMA is subsequently dosed on the surface forming and ordered monolayer of Al-O-Si bonds. STS indicates this unpins the Fermi level, leaving an electrically passive ordered layer which serves as an ideal template for further high-k ALD.

4:20pm **EM+2D-TuA7 Interfacial and Electrical Study of Crystalline Oxidation Passivation for AlGaN/GaN HEMTs**, ***Xiaoye Qin***, *H. Dong, J.Y. Kim, R.M. Wallace,* University of Texas at Dallas

AlGaN/GaN high electron mobility transistors (HEMTs) are of significant interest for high power, high frequency and high temperature devices. However, these are known to experience significant surface related effects, such as large leakage currents and frequency dependent current collapse. Oxidation has been found to have a variety of effects on the atomic and electronic structure of nitride surfaces. Therefore, the oxidation layer and the device performance are closely related. Typically, GaN and AlN are found to form a disordered oxide layer related to high density of states when exposure to with O_2. Miao *et al.*[1] reported that oxidation of AlN and GaN surface change the density of surface states based on density functional theory (DFT). In their work, a 2 ML crystalline oxide can cause the lowest density of surface states within the band gap. However, experimental evidence of a 2 ML crystalline oxide remains to be established.

In this study, we investigate O_2 plasma- exposed AlGaN surfaces at 300 °C and 550 °C by *in situ* X-ray photoelectron spectroscopy (XPS), low energy electron diffraction (LEED). The results indicate that a 500°C O_2 remote plasma exposure is able to generate a thin 2 ML ordered oxide on AlGaN surface and the oxide is stable during subsequent ALD processing, in contrast to arsenide surfaces.[2] The capacitance- voltage (C- V) results indicates that the 2 ML crystalline oxide reduces the D_{it} and shifts the threshold voltage to positive voltages. The I-V and gate leakage current characteristics for crystalline oxide MOSHEMTs will also be presented. This work is supported by the AFOSR Asian Office of Aerospace Research and Development (AOARD) under Grand No. FA2386- 11- 1- 4077.

References

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4:40pm **EM+2D-TuA8 Investigating Electrically Active Defects in High-*k*/InGaAs MOS System using MOS Capacitors and MOSFETs**, ***Paul Hurley***, Tyndall National Institute, Ireland, *V. Djara*, IBM Research - Zurich, Switzerland, *E. O'Connor, S. Monaghan, I.M. Povey, J. Lin*, Tyndall National Institute, Ireland, *M.A. Negara*, Stanford University, *B. Sheehan, K. Cherkaoui*, Tyndall National Institute, Ireland **INVITED**

As silicon devices reach the limit of dimensional scaling there is a growing interest in the use of high electron mobility channels, such as $In_xGa_{1-x}As$, in conjunction high dielectric constant (high-*k*) gate oxides for *n*-channel Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs) and tunnel FET (TFETs) based devices. The understanding and control of electrically active defect states at the high-*k*/$In_xGa_{1-x}As$ interface and of charges within the atomic layer deposited (ALD) high-*k* films will be essential for the successful implementation of high mobility channel materials. The objective of this presentation will be to provide an overview of the current understanding of the density and distribution of electrically active defects at the high-*k*/InGaAs interface both within the InGaAs energy gap and extending into the InGaAs conduction band. The presentation will focus on InGaAs with a 53% Indium concentration. The electrically active interface state density distribution is determined from fully fabricated InGaAs MOSFET structures based on the full gate capacitance in conjunction with the Maserjian Y-function and Poisson-Schrodinger simulations. Very significant progress has been made in recent years in the passivation and intrinsic elimination of high-*k*/$In_{0.53}Ga_{0.47}As$ interface defects to the point where genuine surface inversion for *n* and *p* type InGaAs MOS structures can be achieved and this research will be reviewed. The characteristic signatures of capacitance and conductance for an InGaAs MOS structure in inversion will also be discussed.

Electrically active defects with energies aligned with the InGaAs conduction band are significant for surface inversion mode MOSFETs and can result in a partitioning of charge between free carriers and trapped charge for devices biased above the threshold voltage. The presence of such defect also complicates the extraction of free charge and carrier mobility from device analysis. In this presentation we will also review a new approach where the technique of inversion charge pumping (initially developed for silicon MOSFETs) is applied to InGaAs MOSFETs to determine the free carrier concentration. Results will also be presented which indicate that the duty cycle of the inversion charge pumping technique can be used to discriminate between fast interface states and traps within the oxide for InGaAs MOSFETs biased beyond the threshold voltage.

5:20pm **EM+2D-TuA10 XPS Study of High-k Gate Stack and Interaction with Different Channel Materials and Metal Gate**, ***Malcolm Bevan***, Applied Materials Inc. **INVITED**

Deposited high-k dielectrics with metal gates have replaced SiON gate with poly electrodes for several Logic nodes and rapidly followed with integration changes from planar to 3D FINFET structures. Performance is no longer through just scaling, and next generation devices have gaps that are being addressed with channel engineering using high mobility materials such as SiGe, Ge and III-V compound semiconductors. Gate stacks now involve several thin films of dissimilar material whose interfaces need to be precisely controlled as well as being conformal around the fin and between the spacers. The stack usually involves the channel material followed by a thin interface layer(iL), high-k dielectric and metal gate cap(MG cap) and each layer range from 0.5 to 2nm. In addition several layers may need plasma or thermal treatment to improve reliability and BTI of the gate stack. To understand performance of these stacks, XPS has been applied to compliment device results. In Fab XPS is a powerful tool to provide in short time information on stack thickness, composition and changes in bonding. Examples will be given to show how XPS has been used to optimize and compare high-k stack on Si, SiGe and Ge. In addition iL/high-k/TiN cap has been studied and further examples given and related to electrical device results.

6:00pm **EM+2D-TuA12 Reliability of nc-CdSe Embedded ZrHfO High-*k* Dielectric Nonvolatile Memory – Temperature Effects**, ***Shumao Zhang***, *Y. Kuo*, Texas A&M University

Previously, it was reported that by adding the third element into the high-*k* film, the bulk and interface material and electrical properties can be improved [1]. For example, the Zr-doped HfO_2 film (ZrHfO) shows the higher crystallization temperature, a lower interface state density, and a larger effective *k* value than those of the un-doped HfO_2 film [1,2]. Furthermore, nanocrystals have been embedded into this kind of high-*k* film for the nonvolatile memory (NVM) application to replace the conventional floating-gate flash memory due to the improved device characteristics and reliability [3]. The nanocrystalline cadmium selenide (nc-CdSe) embedded ZrHfO MOS capacitor has shown excellent charge trapping and retention capabilities [4]. However, most studies on the nanocrystals embedded high-*k* memory devices are done at the room temperature. Since the temperature in the high density integrated circuit can be much higher than room temperature, it is imperative to study the reliability at a raised temperature [5]. In this paper, the temperature effects on memory functions were investigated on the nc-CdSe embedded sample in the range of 2 0°C to 120°C. Compared with the fresh *C-V* curve, the flat band voltage (V_{FB}) of *C-V* curve shifts to the negative or positive gate voltage (V_g) direction after being stressed at -6 V or +6 V for 10 s, respectively. With the increase of the temperature, the magnitude of the V_{FB} shift increases at -6 V stress but decreases at +6 V stress. With the increase of the temperature, the hole-trapping is enhanced due to the increase of injection and retention of holes to the trapping sites. However, at the high temperature, electrons are possibly transferred through the whole high-*k* stack with minimum trapping to the high-*k* stack. In addition, at the high temperature, the nc-CdSe embedded sample has the large relax current with the high discharge rate due to the increasing release of the trapped charges with large thermal energy. The charge retention capability of the device decreases with the increase of the temperature. For example, the device stressed at -6 V for 20 s will retain 30% of the original trapped holes at 20°C, 23% at 70°C, and 15% at 120°C, respectively, after 10 years. This is because the stored charges gain the high thermal energy and the bulk high-k film is more conductive at the high temperature.

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