Nanomanufacturing Science and Technology Focus Topic
Room: 16 - Session NM+NS+MS+EM-MoA

ALD and Scalable Processes for Nanomanufacturing

Moderator: T.S. Mayer, Penn State University

2:00pm **NM+NS+MS+EM-MoA1 From R&D Towards Industrial Atomic Layer Deposition: Challenges in Scaling up**, ***M. Putkonen***, Beneq Oy, Finland

More and more ALD-enabled applications are emerging. Most of the ALD processes and applications are first demonstrated by small scale experiments. In optimal cases, the innovations lead to material-application combinations which have solid commercial interest. In the subsequent verification and pilot production phase, there is need for increased throughput and reduced costs also for the ALD processed materials.

There are two main features of ALD, that should be optimized when industrial scale production is being considered. Firstly, in large-area coating processes, more attention should be paid to the properties of the precursors. For large-area coatings, large doses of precursors are delivered to the substrates, preferably in very short pulses in order to keep the total cycle time as short as possible. This often requires either DLI-type sources or increased vapor pressure (i.e. increased thermal stability of metal precursors). In addition, although the ALD chemistry should be surface controlled and not dependent on the substrate surface area, deposition rates and film uniformities are habitually dependent on the tool configuration.

Secondly, ALD has so far been largely confined to laboratories due to non-availability of efficient, larger scale, high-throughput ALD systems. Whereas sputtering and CVD have been mainstream coating tools for decades, ALD has only recently started to gain acceptance as a mainstream industrial coating method. For example, ALD is widely seen as the desired manufacturing technology for producing high-quality functional layers for solar cells and packaging materials, but ALD is commonly considered too slow for high throughput manufacturing. However, large-area batch ALD tools, such as the Beneq P800, can operate up to 10 m^2 batch sizes and still maintain ALD cycle times in the range of 3-5 s. Currently, industrial ALD is diffusing into various industrial thin film areas where single wafer, batch or roll-to-roll ALD is the preferred coating method.

In this presentation, we discuss the different requirements for single wafer, conventional batch, cross-flow batch as well as spatial ALD deposition processes and tools for large throughput applications. In addition to conventional Al_2O_3 and TiO_2 processes, SiO_2 processes are used as examples when scaling up chemistry from single wafer to batch ALD. In addition, process transfer from an R&D scale Beneq TFS 200R rotating drum reactor to the true roll-to-roll Beneq WCS 500, developed for OLED encapsulation applications, is discussed in detail. Results of the studies using this system are presented including temperature dependence of growth rate, RI and WVTR measurements.

2:20pm **NM+NS+MS+EM-MoA2 Enabling ALD for Semiconductor Manufacturing**, ***D. Chu***, Applied Materials Inc. **INVITED**

Atomic layer deposition (ALD) is being extensively studied for semiconductor applications because of its precise, atomic level thickness control for very thin films; ALD is extremely conformal and the overall thermal budget is lower than its CVD alternatives. However, ALD is inherently slow which makes it cost prohibitive.

Adoption of ALD processes into manufacturing requires consideration of multiple factors. At Applied Materials, we focus on three main areas to enable ALD for volume manufacturing.

1. Atomic level engineering to create differentiated solutions that boost device performance.

2. Tool architecture and methods to allow integration of multiple films without vacuum break. This is particularly of importance when films scale to Angstrom level, stability of the film becomes an issue. Extendable tool architectures allow integration of other films such as capping layers and pre-post treatments to address this issue

3. Accelerate adoption of standalone ALD films by improving manufacturability and productivity while maintaining single wafer performance

Example applications and challenges for each area will be discussed in this paper.

3:00pm **NM+NS+MS+EM-MoA4 Migration to ALD Techniques in the Semiconductor Industry: Pattern Effects, Microloading and Film Thickness Variability in Dielectric Thin Films Deposition**, ***M.P. Belyansky***, IBM Semiconductor R&D Center

The continuation of scaling in the microelectronics industry is having a profound effect on thin film deposition techniques and processes. One of the consequences of the scaling is a decrease in average film thickness to accommodate the shrinking device dimensions which amplifies the problem of film thickness variability. Most of the CVD deposition techniques and tooling are reaching the limit of reliable thickness control of very thin films. At the same time, circuit designs are becoming more complex, which leads to significant pattern density variation on macro scale. Therefore CVD technology is facing a tremendous challenge in controlling film thickness and properties across variable pattern density which has been one of the major reasons that facilitated the transition to ALD-like deposition techniques and processes in the industry.

The paper discusses the microloading effect (dependence of thin film deposition rate on pattern density) as well as other manifestations of pattern effects in the semiconductor manufacturing. The data shows the effect of microloading on the variation of as deposited film thickness across features of different size as well as for identical features with different pattern density in the surrounding areas. The microloading performance of CVD and ALD silicon oxide and silicon nitride dielectric thin films is covered as well as methods aimed at quantifying and improving thin film variability. The effects of major process parameters, precursor chemistry and tool design on the thin films microloading performance are delineated. Thin films step coverage over a nano scale feature and pitch to pitch film thickness dependence for CVD and ALD dielectric processes are also discussed.

3:40pm **NM+NS+MS+EM-MoA6 Interface Analysis of PEALD TaCN Deposited on HfO_2 using Parallel Angle Resolved X-ray Photoelectron Spectroscopy for sub-20nm Gate Last CMOS Transistors**, ***F. Piallat***, ST Microelectronics, France, *V. Beugin, R. Gassilloud, P. Michallon,* CEA Grenoble, France, *L. Dussault, B. Pelissier,* LTM - MINATEC - CEA/LETI, France, *C. Leroux,* CEA Grenoble, France, *P. Caubet,* ST Microelectronics, France, *C. Vallée*, LTM - MINATEC - CEA/LETI, France

Sub-20 nm high-k/metal CMOS devices require about 2 nm thin metal gate electrode with adapted work function (WF) and chemical inertness regarding the high-k dielectric sub-layer. TaCN material deposited by Plasma Enhanced Atomic Layer Deposition (PE-ALD) has been investigated as a possible gate electrode candidate [1-2]. Depending on the carbon content TaCN can presents a *p-type* behavior with a WF from 4.5 to 4.7eV [3]. Besides plasma used for deposition may have an impact on the under-layer dielectric such as an increase of the EOT [4]. A deviation from bulk material characteristics of the metal gate WF is induced by the intimate bond linking environment at high-k/TaCN interface, but these chemical mechanisms are still unclear. Thus, in this work, interface of TaCN and HfO_2 dielectric is carefully analyzed by X-Ray Photoelectron Spectrometry (XPS), using Ta4f, Hf4f, O1s, C1s, N1s and Si2p core levels, and obtained bonding environments are correlated to work function extracted from MOS capacitors.

Thanks to chemical stability of SiO_2 [5], bonding environments of $TaCN/SiO_2$ and HfO_2/SiO_2 stacks were chosen as reference for XPS analysis. Then, by comparing TaCN deposited on HfO_2 spectra with these references, the evolution of the chemical environments can be determined, thus a mechanism of interaction between the two materials is proposed. Furthermore, it appeared that, when deposited on HfO_2, TaCN oxidation is higher than on SiO_2, which is attributed to the higher capacity of HfO_2 to have O deficiency [6].

In addition, $TaCN/HfO_2/SiO_2$ stack was measured using Parallel Angle Resolved XPS (PARXPS) in order to build a depth composition profile. This profile confirms the modifications of chemical environment such as oxidation of the electrode close to high-k/metal interface, it also shows N penetration in HfO_2, which could be induced by plasma densification.

Finally, electrical results from MOS capacitors with $TaCN/HfO_2/SiO_2$ stacks and TiN/W plug have shown an evolution of the *p-like* metal flat band voltage (Vfb) with plasma conditions. The modifications of chemical bonding environment observed at the high-k/metal interface can give insight on this deviation of Vfb with plasma.

[1] W. S. Hwang, D. Chan, B. Jin Cho, IEEE Transactions on Electron Devices, 55, (2008)

[2] H. Zhu and R. Ramprasad, Journal of Applied Physics 109, 083719 (2011)

[3] H. N. Alshareef, et al., Electrochemical and Solid-State Letters, 11, H182 (2008)

[4] H. C. Shin and C. Hu, Semiconductor Science Technologie, 11, 463, (1996)

[5] M. Zier, et al., Applied Surface Science 252, 234 (2005)

[6] G. D. Wilk, R. M. Wallace and J. M. Anthony, Journal of Applied Physics 89, 5243 (2001)

4:20pm **NM+NS+MS+EM-MoA8 Atmospheric Pressure Atomic Layer Deposition of Al_2O_3 using Trimethylaluminum and Ozone**, ***M.B. Mousa***, *D.H. Kim, C.J. Oldham, G.N. Parsons*, North Carolina State University

Atomic layer deposition (ALD) is used for nanoscale coatings with high uniformity and precise thickness control. Currently, most commercial ALD processes operate in batch mode. Expanding to ambient pressure can increase throughput and facilitate its integration for applications such as smart textiles, flexible electronics and synthetic polymer coatings. We find that under certain flow conditions in the trimethylaluminum (TMA)/water ALD process for Al_2O_3, increasing the reactor pressure from ~ 2 Torr to 760 Torr can produce excess film growth per cycle.

For this work, we studied ALD of Al_2O_3 using TMA/O_3 and compared growth at ~ 2 Torr to that at 760 Torr in a flow tube reactor. We measured film thickness by ellipsometry and surface morphology by AFM. Also, we plan to monitor in-situ growth using a quartz crystal microbalance (QCM). At 2 Torr, by changing the ozone and TMA exposure times, we saw clear ALD saturation at ~ 0.45 Å/cycle at 170°C. A shorter purging time after the ozone exposure tends to increase the growth per cycle. Deposition at higher pressure results in growth rates between ~0.3 and 0.6 Å/cycle at 205°C, with lower growth rates obtained under higher gas flow rate conditions. For both the water and O_3 processes at 760 Torr, a low gas flow rate of 0.5 standard liters per minute (slm) in our flow-tube reactor leads to a high growth rates of ~3 Å/cycle (for water) and 0.6 Å/cycle (for O_3). For the water process at 760 Torr, increasing the flow rate to 10 slm somewhat decreases the growth per cycle to ~1.35 Å /cycle. However, for the O_3 processes at 760 Torr, we need only a relatively small increase to 1.5 slm to achieve growth of 0.3 Å/cycle. This could be due to enhanced ozone desorption kinetics compared to the rate of water desorption under the conditions used. Also interestingly, we find for the water process that films deposited at high pressure have higher surface roughness than films deposited at low pressure. These results will help to identify the key parameters for new continuous atmospheric pressure ALD reactors designs.

4:40pm **NM+NS+MS+EM-MoA9 An Industrial Solution for Surface Passivation of c-Si using AlO_x Film Deposited by In-line Atmosphere Chemical Vapor Deposition**, *K. Jiang*, Gebr. Schmid GmbH + Co, Germany, ***K.O. Davis***, University of Central Florida, *C. Demberger, H. Zunft, H. Haverkamp*, Gebr. Schmid GmbH + Co, Germany, *W.V. Schoenfeld*, University of Central Florida, *D. Habermann*, Gebr. Schmid GmbH + Co, Germany

Among the different dielectric passivation layers for crystalline silicon (c-Si) solar cells, AlO_x has recently received a great attention due to its excellent chemical and field effect passivation performance for p-type c-Si surface. It offers great promise as a rearside passivation material for passivated emitter and rear cell (PERC) designs. However, up to this point in time, most of the development has been based on laboratory scale deposition systems and methods. Common approaches for synthesizing these passivation layers are thermal or plasma-assisted atomic layer deposition (ALD), whose deposition rates are typically too low (< 10 nm/min) to be compatible with high-volume manufacturing. Other deposition methods like PECVD or spatial separated ALD enable an increase in deposition rate by one order of magnitude (i.e. 100 nm/min). An industrially-compatible deposition technique with low processing cost, easy-handling, compact size, and high throughput that still retains comparable passivation performance to ALD films remains a challenging task.

Using an in-line atmosphere chemical vapor deposition (APCVD) tool, we have synthesized amorphous AlO_x films from precursors of trimethylaluminum and O_2, yielding a maximal deposition rate of up to 150 nm/min per wafer. Deposition rate is determined by the film thickness divided by wafer transportation time through the CVD injector. Both top view and the cross-sectional SEM images present an intact AlO_x/Si interface. A smooth surface is shown without any outgassing (blistering) after deposition and a subsequent firing step. The as-deposited layers exhibit an over stoichiometric O/Al ratio of 1.65~1.75 due to the incorporation of an OH group inside the layer. For both high and low doped p-type c-Si wafers deposited with APCVD AlO_x, excellent surface passivation is achieved with a maximum effective surface recombination velocities ($S_{eff,max}$) of 8 cm/s following by a firing step. These findings are attributed to the buildup of a large negative charge ($Q_f \approx -3 \times 10^{12}$ cm^{-2}) and low interface defect density ($D_{it} \approx 4 \times 10^{11}$ eV^{-1}cm^{-2}) following the firing process. It is believed that the incorporated OH group plays an essential role during the firing step. During the annealing/firing step, a certain degree of dehydration takes place (i.e. Al sites bonded OH termination start to bond via an O bridge), which may involve an octahedral to tetrahedral coordination change. This could facilitate the negative charge formation and release of atomic H for passivating the Si dangling bonds at the AlO_x/Si interface.

This data implies a high application potential of APCVD AlO_x for low cost industrial solar cell applications.

5:00pm **NM+NS+MS+EM-MoA10 Solution Based Processing of Floating Gate Memory using Additive-Driven Self-Assembly and Nanoimprint Lithography**, ***J. Watkins***, University of Massachusetts **INVITED**

Polymer and polymer-inorganic hybrid materials organized at the nanoscale are at the heart of many devices that can be created on flexible substrates for applications in energy generation and storage, microelectronics, optoelectronics, communications and sensors. The challenge is to produce these materials using process platforms and materials sets that are environmentally and economically sustainable and can be scaled for cost-effective, high value-added manufacturing. Here we describe a resource efficient, additive approach based on roll-to-roll coating of self-assembled hybrid materials. Specifically we report that nanostructured templates with periodic spherical, cylindrical, and lamellar morphologies exhibiting sub-10 nm domains can be easily obtained through the blending of commercially available disordered polymer surfactants with commodity homopolymers that selectively associate with one segment of the surfactant. We further demonstrate that order in the surfactant systems and in block copolymer templates can be induced by nanoparticle additives that undergo multi-point hydrogen bonding with one of the segments of the polymer template. These additives, which include metal and semiconducting nanoparticles, fullerenes, and other active components, impart functionality to the device. The strong interactions further enable particle loadings of more than 40% in the target phase, resolving a crucial constraint for many applications. These systems can be scaled in our newly constructed R2R processing facility, which includes a custom microgravure coater for hybrid materials that is equipped for in-line substrate planarization and a precision R2R UV-assisted nanoimprint lithography (NIL) tool.

We illustrate the capabilities of these approaches by the fabrication of floating gate field effect transistor memory devices. For this application, the charge trapping layer is comprised of well-ordered polymer/gold NP composites prepared via additive-driven self-assembly; the addition of gold nanoparticles that selectively hydrogen bond with pyridine in poly(styrene-*b*-2-vinyl pyridine) copolymers yields well-ordered hybrid materials at gold nanoparticle loadings of more than 40 wt.%. The charge trapping layer is sandwiched between a dielectric layer and a poly(3-hexylthiophene) semiconductor layer. We can achieve facile control of the memory windows by changing the density of gold nanoparticles. The devices show high carrier mobility (> 0.1 cm^2/Vs), controllable memory windows (0~50V), high *on/off* ratio (>10^5) between memory states and long retention times. Strategies for patterning of the device using NIL will be discussed.

Authors Index

Bold page numbers indicate the presenter