Thursday Morning, November 1, 2012

Electronic Materials and Processing
Room: 9 - Session EM-ThM

Processing for Ultra Low Power Electronics + Semiconductor Heterostructures I
Moderator: S.A. Vitale, MIT Lincoln Laboratory, J.E. Ayers, University of Connecticut

8:00am **EM-ThM1 Advanced FinFET Process for 22nm and Beyond**, ***M. Masahara***, *T. Matsukawa, Y. Liu, K. Endo, S. O'uchi*, National Institute of AIST, Japan **INVITED**

1. Introduction

One of the biggest challenges for the VLSI circuits with 22nm-node and beyond is to overcome the issue of a catastrophic increase in power dissipation of the circuit due to short channel effects (SCEs) and Vth variation. Fortunately, double-gate FinFETs have a promising potential to overcome this issue due to their superior SCE immunity even with an undoped channel thanks to the 3D structure. This paper presents novel FinFET process technologies for 22nm-node and beyond.

2. Vth Tuning

The Vth of the FinFET is determined by the gate workfunction (WF). A mid-gap metal gate (MG) such as TiN gives a relatively high Vth (±0.4V) for both n- and pMOS FinFETs. In order to further reduce Vth, we have developed a novel dual MG FinFET integration process by using metal interdiffusion technology. In this work, we selected a Mo (4.95eV) and Ta (4.25eV) combination, and demonstrated the integration of a Ta/Mo gate nMOS and Mo gate pMOS FinFET. A Ta diffuses into the underlying Mo layer, piles up at the metal/dielectric interface. Thus, by depositing Mo on both n- and pMOS and by stacking Ta on only pMOS, dual MG CMOS FinFETs with low Vth (±0.2V) were successfully realized without any MG removal process.

By separating the two gates in the FinFET and using one to control the Vth, we have succeeded in obtaining the great advantage of the post-fabrication flexible Vth controllability. The fabricated independent double-gate FinFET (called 4T-FinFET) enabled Vth to flexibly range from around 0.2V to 0.4V.

3. Vth Variation

So far we have investigated FinFET performance variability for undoped channels with TiN MG. By evaluating the influence of channel doping, fluctuation of gate length and that of fin thickness, we have also found that gate WF variation (WFV) is the dominant source of Vth variation for the undoped TiN FinFET. We speculated that the WFV originates from randomly aligned TiN on rough sidewall channels due to line edge roughness of the patterned resist mask. Then in order to reduce the WFV, we fabricated FinFETs having smooth sidewall channels formed by using orientation-dependent nanowet etching. It was found that σVth's for the wet-etched case is significantly lower than that for the dry-etched case. This means that the smooth sidewall channels formed by using the nanowet etching well contribute to the reduction of the WFV.

4. Summary

By introducing Ta/Mo dual metal gate technology, low Vth (±0.2V) can be obtained for CMOS FinFETs. By separating the DG, Vth can be tuned from 0.2V to 0.4V flexibly. Flattening of Si-fin sidewall channel is very promising for reducing Vth variations.

9:00am **EM-ThM4 Wideband Characterization for Optimized Performance in Low Voltage Low Power Applications**, ***M. Emam***, Incize, Belgium, *J.-P. Raskin*, Université Catholique de Louvain, Belgium

Portability and performance are becoming the main two keywords in any consumer or professional applications. Portable computers, mobile phones, handheld measurement instruments, and many other examples are all applications that need long battery lifetime while compromising the least at the performance level. Long battery lifetime is simply translated into less power consumption and hence operating at lower voltage schemes. This new approach requires solutions at all levels; including material, fabrication, device structure, circuit design, and system architecture. Wideband characterization is the bridge that links these levels together (especially material, fabrication and device structure levels) and provides the means to optimize this cycle of innovation for an optimized final product in the Low Voltage Low Power (LVLP) regime.

Wideband characterization is the process of measurement and extraction of many parameters of the Device-Under-Test (DUT) in order to fully understand its characteristics and be able to provide solutions for inconvenient performance aspects. Wideband characterization usually covers a wide range of frequency starting at a few Hz and going up to tens of GHz, depending on the characteristics to be studied. Recently, many high frequency techniques have been proposed to deeply understand and qualify new materials (especially wafers and substrates) and new devices (active devices such as transistors and passive devices such as inductors). These new techniques rapidly and efficiently define the advantages and the disadvantages of the material/device and precisely define the causes of malfunction or poor quality performance. The result is a shorter time-to-market thanks to less number of iterations between the different steps of final product fabrication.

This paper presents the importance of wideband characterization techniques for fabrication process. Examples are given for new substrate, new device structures and enhancement of existing and mature device structures. The objective is an optimized performance for a LVLP application.

9:20am **EM-ThM5 Ultra Low-Power (ULP) Current Logic Gates for Subthreshold-Triode Operation**, ***K. Lam***, Chinese University of Hong Kong, Hong Kong Special Administrative Region of China, *T. Mak*, Newcastle University, UK

Most logic gates used today are based on voltage-mode ideas, where the two binary states for 0 and 1 are represented using inverted logic on voltages. In carrying out the basic operations for AND and OR on two levels of voltages for 0 and 1, NAND gates and NOR gates are often required by using inverted logic and inverters are commonly used to get the logical computations functionally correct. It is straightforward to construct a NAND gate with two tightly coupled common drain and source N-channel MOSFET transistors. A properly chosen resistor from the supply voltage to the common drain will then realize the NAND function to the two voltage levels with a reasonable margin. For subthreshhold operation with a supply voltage close to the threshold voltage, the gate switching speed is determined by the subthreshold swing.

There are limitations for these voltage-mode logic gates due to the lack of accuracy and inability to work on very small voltage levels less than the threshold voltage for ultra-low power applications. We explore the idea of current logic by making use of small currents at the subthreshold-triode region to overcome some of these limitations. Using current for the binary inputs of 0 and 1, the 2-input current-mode minimum circuit and maximum circuit are investigated to realize the logical functions of OR and AND gates for subthreshold-triode operation. Our previous work reported that in subthreshold-triode operation it is possible to obtain a subthreshold swing which can surpass the theoretical limit of 60 mV/dec at very small gate voltage less than 0.025V for the IMEC 90 nm process. Further simulation is focused on the evaluation of ULP current logic gates constructed using current-mode min-max circuits. A benchmark test on a dynamic programming network for solving transitive closure problem has been performed on using conventional voltage-mode NAND-NOR logic gates. The results will be compared with the proposed current-mode min-max circuits.

9:40am **EM-ThM6 Impact of Threading Dislocation Density and Dielectric Layer on I-V Characteristics of Schottky Diodes Fabricated from Ti and Epitaxially Grown p-Type Ge on Si**, ***S. Ghosh***, *S.M. Han*, University of New Mexico

Epitaxially grown Ge and III-V on Si have emerged as a promising candidate for the next generation high performance devices, including high-mobility complementary metal-oxide-semiconductor field-effect transistors. For high-mobility transistors integrated on Si substrates, in particular, managing dislocations and metal-semiconductor contacts has become an important engineering challenge. Herein, we have investigated the impact of threading dislocations and metal-semiconductor interfacial states on Schottky diode characteristics made of Ti and wafer-scale Ge grown on Si. For the purpose of comparison, we have grown epitaxial Ge on Si with two threading dislocation densities: $2x10^8$ and $5x10^7$ cm^{-2}. The p-type carrier density in the Ge layer is approximately $5x10^{16}$ cm^{-3}. To prevent Fermi-level pinning, we have also deposited a thin layer of SiO_2 and Al_2O_3 between Ti and Ge with varying thickness, ranging from 5 to 30 nm. With a thin dielectric layer (5 nm), Schottky diodes on two Ge epilayers resulted in an on/off current ratio of approximately 1. This result indicates that there is a significant amount of leakage current. When the dielectric thickness is optimized to 30 nm, we observe that the on/off ratio improves by a factor of 40 and 2000 for SiO_2 and Al_2O_3, respectively. In the case of Al_2O_3, we were able to achieve an ideality factor of 1.67 at 300 K and the reverse leakage current density of ~$4.3x10^{-10}$ A/μm^2 at 300 K. The ideality factor increases to 2.44 at 77 K. This result suggests that the thermionic emission might be the dominant current transport mechanism for Schottky diodes fabricated

from Ti and epitaxially grown p-type Ge on Si. However, the slight increase in ideality factor at low temperatures implies a change in the dominant current transport mechanism. In summary, the use of 30-nm-thick Al_2O_3 between Ti and Ge provides improved I-V characteristics for the Schottky diodes. In this presentation, we will further discuss our latest approaches[1] to reduce the dislocations in the Ge epilayer to low 10^6 cm^{-2} level and device characteristics of Schottky diodes fabricated on these low-dislocation-density Ge on Si substrates.

[1] Darin Leonhardt and Sang M. Han, *Appl. Phys. Lett.* 99, 111911 (2011).

10:40am **EM-ThM9 Heteroepitaxial Lattice Mismatch Stress Relaxation in Nonpolar and Semipolar GaN by Dislocation Glide**, ***J. Speck***, University of California, Santa Barbara **INVITED**

Light emitting devices, namely LEDs and laser diodes, grown on *c*-plane GaN suffer from large internal electric fields due to discontinuities in spontaneous and piezoelectric polarization effects which cause charge separation between holes and electrons in quantum wells and limits the radiative recombination efficiency. Nonpolar GaN devices, such as in the *m*-plane {1100}, are free from polarization related electric fields since the polar *c*-axis is parallel to any heterointerfaces. Semipolar GaN-based devices have reduced electric fields.

Nonpolar and semipolar nitride epitaxial layers have other striking differences from c-plane. Namely, in conventional c-plane GaN heteroepitaxy, there is no shear stress on the easiest slip plane – the (0001) or basal plane and the next easiest slip plane – the prismatic {1100} m-plane. Epitaxy of mismatched layers on nonpolar and semipolar GaN, there are significant shear stresses in the inclined m-planes and on the inclined c-plane. Significant lattice mismatch-related stresses can be relieved by misfit dislocation formation via threading dislocation glide.

In this talk, we present the progress in developing high quality relaxed semipolar templates. The predominant relaxation in semipolar InGaN on GaN or AlGaN on GaN, in orientations such as (1122) or (2021), proceeds via threading dislocation glide on the inclined basal plane, followed in many cases by prismatic slip [1]. Since semipolar GaN has only one (0001) plane, plastic relaxation results in crystallographic tilt which can easily be measured in on-axis x-ray rocking curves or reciprocal space maps and can be directly used to quantify the extent of plastic strain relaxation [2]. The initial misfit stress relaxation occurs by glide of pre-existing threading dislocations [3,4] at a thickness slightly greater than the Matthews-Blakeslee critical thickness; the development of pseudomorphoric InGaN and AlGaN semipolar buffer layers via dislocation strain relaxation [5,6,7]; blue (1122) LDs in relaxed buffer layers [8]; green LEDs on relaxed buffer layers [9].

[1] F. Wu et al., *Appl. Phys. Lett* **99**, 251909 (2011).

[2] E.C. Young et al. *Appl. Phys. Express* **3**, 011004 (2010).

[3] E.C. Young et al. *Appl. Phys. Express* **3**, 111002 (2010).

[4] P.S. Hsu et al., *Appl. Phys. Lett.* **99**, 081912 (2011).

[5] F. Wu et al. *J. Appl. Phys*. **109**, 033505 (2011)

[6] A.E. Romanov et al., *J. Appl. Phys*. **109,** 103522 (2011).

[7] E.C. Young et al. *Appl. Phys. Express*, **4**, 061001 (2011).

[8] P.S. Hsu et al. *Appl. Phys. Lett.* **100**, 021104 (2012).

[9] I. Koslow et al. submitted for publication (2012).

11:20am **EM-ThM11 Electronically Unmixed State of a Statistical Two-Dimensional Ga-Si Semiconductor Alloy on Si(111)**, ***P. Ebert****, S. Landrock,*** Forschungszentrum Jülich, Germany*, Y. Jiang,* Peking University, China*, K.H. Wu,* Chinese Academy of Sciences, China*, E.G. Wang,* Peking University, China*, R.E. Dunin-Borkowski*, Forschungszentrum Jülich, Germany

Alloying different semiconductor compounds attracted wide attention, since the materials properties of the resulting semiconductor alloy can be continuously tuned by varying the composition. Hence one can engineer semiconductor materials with, e.g., intentionally designed band gaps, lattice constants, and/or optical properties. This approach possesses a large technical and economical interest, as it is the basis for defining the wavelength of most optoelectronic devices.

For such applications, it is crucial that the newly formed semiconductor alloy has spatially homogeneous electronic properties, i.e., the original materials' properties of the individual alloyed compounds merge into the desired new properties. This is in general assumed to be the case for most three-dimensional compound semiconductor alloys. With the ever shrinking dimensions of semiconductor devices, the semiconductor alloy layers are be coming increasingly thinner. Ultimately only monolayer thin alloy layers may be needed and then the concept of a globally homogenous alloy band structure, different from that of its alloyed compounds, needs to be reassessed. The central question is if a two-dimensional semiconducting alloys would always exhibit a merged new band structure in analogy to three-dimensional semiconductor alloys, or if locally the different band structures of the constituent semiconductor compounds of the alloy persist.

In this paper, we present a two-dimensional Ga-Si $\sqrt{3}x\sqrt{3}$ semiconductor alloy on Si(111) substrates as model system. Using atomically and momentum resolved STM and STS, we demonstrate that the electronic structure, i.e., density of states, band gap, and band structure, is atomically localized and different at Si and Ga atoms. No intermixing and formation of new alloy related electronic properties are observed, as if no alloying ever happened. This unmixed state is discussed in terms of the particular bonding structure of the two-dimensional alloy.

11:40am **EM-ThM12 Atomistic Analysis of Ge on a-SiO_2 using an Emipirical Interatomic Potential to Describe Selective Epitaxial Growth**, ***Y. Chuang****,*** University of Pennsylvania*, Q. Li, D. Leonhardt, S.M. Han,* University of New Mexico*, T. Sinno*, University of Pennsylvania

Integration of Ge and III-V compound semiconductors on Si has received significant recent attention for the next-generation, high-mobility transistors and III-V optoelectronic and photovoltaic devices.[1] However, managing dislocations and film stress due to lattice mismatch and thermal expansion coefficient mismatch remains a significant engineering challenge. One possible solution is selective epitaxial growth (SEG) where the epitaxial layer is grown in select areas to simultaneously manage dislocations and stress. For SEG, a dielectric layer (e.g., SiO_2 and Si_3N_4) with open windows that expose the underlying Si is typically employed to reduce the contact area between the deposited epitaxial layer and Si substrate, resulting in lower mismatch stress and defect density.[2] The selectively grown epitaxial islands can be further grown laterally over the dielectric layer and coalesced into a continuous film. The SEG technique squarely relies on weak interaction between growth precursors and the dielectric film, which prevents random nucleation. For instance, we have previously reported that desorption and surface diffusion barriers of Ge adspecies on SiO_2 are 0.44 ± 0.03 and 0.24 ± 0.05 eV, respectively.[3, 4] Herein, we present an atomistic analysis of Ge on SiO_2 in order to validate a Tersoff-based model for Si-Ge-O [5, 6]. We compare simulation predictions to detailed experimental data for a variety of properties. In particular, we consider bulk SiO_2 structural parameters as a function of temperature, Si-SiO_2 and Ge-SiO_2 interface energies, and the Ge-on-SiO_2 desorption energy and diffusion behavior. We show that with a single fitting parameter, the potential model provides a good overall description of the Si-Ge-O system, while retaining the highly efficient nature of the Tersoff potential, making it a good choice for larger-scale atomistic studies of Ge-on-Si SEG. We conclude by showing example calculations of stress distributions in epitaxial Ge islands in an SEG system.

[1] H. Lafontaine, D. C. Houghton, N. L. Rowell and G. C. Aers, Appl. Phys. Lett. 69, 1444 (1996).

[2] T. A. Langdo, C. W. Leitz, M. T. Currie, E. A. Fitzgerald, A. Lochtefeld and D. A. Antoniadis, Appl. Phys. Lett. 76, 3700 (2000).

[3] Q. Li, J. L. Krauss, S. Hersee, and S. M. Han, J. Phys. Chem. C 111, 779 (2007).

[4] D. Leonhardt and S. M. Han, Surf. Sci. 603, 2624 (2009).

[5] J. Tersoff, Phys. Rev. B 39, 5566 (1989).

[6] S. Munetoh, T. Motooka, K. Moriguchi and A. Shintani, Comput. Mater. Sci 39, 334 (2007).

Authors Index

Bold page numbers indicate the presenter