**Transparent Conductors and Printable Electronics Focus Topic**
**Room: 106 - Session TC+EM+NS-ThA**

**Transparent / Printable Electronics Part 2**
**Moderator:** S. Durbin, University at Buffalo

2:00pm **TC+EM+NS-ThA1 ZnO-based Schottky Diodes and Their Utilization in Transparent Electronics**, ***H. von Wenckstern***, Universität Leipzig, Germany **INVITED**

Transparent conducting oxides (TCO) have found application as electrode in emerging markets like that of thin films solar cells or flat panel displays. For this passive functionality the TCO material must combine high transparency preferentially over a wide spectral range and high conductivity. In the last years active transparent devices like photodetectors, transistors or a complete transparent circuitry are envisioned and rely on semiconducting properties of the material. Besides a precise control of the doping level in the active part of devices the creation of space charge regions by rectifying contacts is a prerequisite for active devices. In the emerging field of transparent electronics, only metal-insulator-semiconductor field-effect transistors (MISFETs) were considered so far. In this contribution transparent, high-performance MESFETs, inverters etc. based on ZnO and related ternaries are presented. We discuss design prospects as well as limitations regarding device performance, reliability and stability.

The influence of the contact metal and dielectric passivation layers on the properties of ZnO Schottky diode, used as gate electrode within the MESFETs, as well as sources of non-idealities will be highlighted.

2:40pm **TC+EM+NS-ThA3 Photoresponse of Amorphous In-Ga-Zn-O / Pt Schottky Junction**, ***D.H. Lee***, *K. Nomura, T. Kamiya, H. Hosono*, Tokyo Institute of Technology, Japan

Amorphous oxide semiconductors (AOSs) are expected as an alternative to amorphous/poly-Si for thin-film transistors (TFTs) in next-generation flat-panel displays (FPDs) because AOS TFTs have many advantages such as large field-effect mobilities (>10 $cm^2(Vs)^{-1}$) and low-temperature process [1]. For more advancing AOS optoelectronic technology, it is important to develop more various devices other than TFTs, and to study some remaining issues such as operation characteristics of AOS devices under light illumination.

In this study, we fabricated good and stable metal-AOS Schottky contacts made of amorphous In-Ga-Zn-O (a-IGZO) and bottom Pt electrodes at temperatures below 200°C even though it is generally difficult to make high performance oxide Schottky junctions [2]. It was found that the a-IGZO/Pt Schottky contacts have an ideality factor n ~ 1.1 and a Schottky barrier height $\phi_b$ ~ 0.9 eV, which were evaluated from their J-V curves using the thermionic emission model. From C-V results, the Schottky junctions operate at the full-depletion condition, whose C corresponds to the geometrical capacitance of the a-IGZO layer, and relative permittivity $\varepsilon_s$ of a-IGZO was obtained approximately 13. However, the results of temperature dependences of J-V characteristics were unexplained if we take a simple uniform Schottky barrier model; we found that the barrier potential fluctuations model [3] explained them well, and the mean barrier height $\phi_{b,m}$ of 1.2 eV and the net electron affinity $\chi_s$ of a-IGZO of 4.2 eV were obtained. On the other hand, the Schottky contacts showed very small open circuit voltages ($V_{OC}$'s) < 0.1 V under 100 $mWcm^{-2}$ AM1.5 light illumination, which are far smaller than the built-in potential ($V_{bi}$ ~ 0.4 eV) estimated from the C-V measurements in dark. We also observed that $V_{OC}$ decays with time after starting the light illumination. We will discuss the mechanism of the small $V_{OC}$ based on these results.

[1] T. Kamiya et. al. *Sci. Technol. Adv. Mater.* **11** 044305 (2010).

[2] K. Ip et al., J. Cryst. Growth **287,** 149 (2006).

[3] J. H. Werner and H. H. Güttler, J. Appl. Phys. **69**, 1522 (1991).

3:00pm **TC+EM+NS-ThA4 Novel Metal-organic Precursors for Printed Electronics - Synthesis, Implementation, and Properties**, ***J.A. Belot***, *R.A. Potash, R.D. McCullough, K.A. Singh, L. Porter*, Carnegie Mellon University

Printed electronics is a rapidly growing industry and within this emerging field there are three required material categories critical to fabricating active and passive circuitry – insulators (dielectrics), semiconductors (polymers), and conductors (metals). The increased interest in printable electronics as alternatives to silicon-based technologies is fueled by the promise of large-area, flexible, and ultra-low-cost devices. To enable the growing demands of printing processes this work develops metal-containing inks for the deposition of the coinage metals - copper, silver, and gold. These metals are chip components ranging from interconnects to source and drain contacts in organic field effect transistors. The liquid ink approach is based on fundamental advances in coordination chemistry to fabricate discrete metal complexes that can be heated or irradiated to yield metallic films. Ultimately inkjet printing technologies were employed to deposit these metal inks in specific, predetermined patterns that were directly transformed into active and passive devices. The versatility of this approach holds the possibility of printing any metallic design and pattern on virtually any type of substrate.

3:40pm **TC+EM+NS-ThA6 A New Application for a-IGZO TFTs: An Addressable Microfluidic Electrowetting Channel Device**, ***J. Noh***, *J.H. Noh*, University of Tennessee, *E. Kreit, J. Heikenfeld*, University of Cincinnati, *P.D. Rack*, University of Tennessee

An electrowetting (EW) microfluidic platform designed for control and transport of aqueous and polar species has been fabricated on passive electrodes as well as an active matrix thin film transistor (TFT) array. To drive the EW devices we integrated the micro fluidic platform on a base-plane of transparent TFTs. Specifically, we have used an InGaZnO (IGZO) active layer for the TFT device which has superior performance and offers the benefit of transparent devices for biological and display applications. The TFTs are fabricated with a bottom-gate staggered structure with Cr gate and SiO2 gate dielectrics deposited via plasma enhanced chemical vapor deposition (PECVD). The a-IGZO semiconducting active layers are deposited using rf magnetron sputtering in a reactive Ar-O2 atmosphere. Finally, source and drain electrodes are formed by e-beam evaporating Ti/Au. Finally the device is annealed in an N2ambient for electrical activation. For the EW device integration, Al electrodes are have been deposited various passivation layers. Subsequently a top dielectric and a hydrophobic Fluoropel layer are applied. In this presentation we will review the process flow and will discuss the materials integration issues of EW device and its effect on the TFT performance. We will illustrate the EW characteristics based on standard planar electrowetting on dielectric (EWOD) platforms and compare them to a new concept we have termed the "Laplace Barrier" which includes post arrays and enhances electrowetting characteristics.

4:00pm **TC+EM+NS-ThA7 Amorphous Oxide Semiconductor Thin-Film Transistors**, ***J.F. Wager***, *K. Hoshino*, Oregon State University, *B. Yeh, R.L. Hoffman*, Hewlett-Packard Company **INVITED**

Amorphous oxide semiconductor (AOS) thin-film transistors (TFTs) are transitioning towards commercialization for active-matrix liquid crystal display flat-panel display backplane applications. They also appear to be well-positioned to meet the more demanding challenges associated with active-matrix organic light-emitting device backplanes. Additionally, AOS TFTs offer an attractive approach to printed electronics. The primary focus of this talk will be to discus our novel approach to top-side passivation of bottom-gate indium gallium zinc oxide (IGZO) and zinc tin oxide (ZTO) AOS TFTs. Device performance between passivated and unpassivated AOS TFTs will be compared. Passivation mechanisms will be considered in the context of induced-gap state and device physics electrostatic modeling.

4:40pm **TC+EM+NS-ThA9 Why Optimum Oxygen Pressure Range Exists for Fabricating Amorphous In-Ga-Zn-O Thin-Film Transistor and How it Should be Optimized**, ***K. Ide***, *K. Nomura, T. Kamiya, H. Hosono*, Tokyo Institute of Technology, Japan

Amorphous oxide semiconductors (AOSs) represented by amorphous In-Ga-Zn-O (a-IGZO) are expected for large-area high-performance flexible electronic devices, because AOSs have large electron mobilities greater than 10 $cm^2(Vs)^{-1}$ even if fabricated at room temperature (RT). In particular, a-IGZO has good controllablities of carrier concentration, and their thin-film transistors (TFTs) exhibit superior properties including long-term stability.

In this study, we investigated effects of oxidation on operation characteristics of a-IGZO TFTs. Bottom gate, top-contact a-IGZO TFTs were fabricated on $SiO_2$/c-Si substrates by RF magnetron sputtering. Sputtering conditions were the RF power of 70 W and the total pressure of 0.55Pa. Two oxidation treatments were examined; (i) ozone annealing and (ii) varying a mixing gas ratio of Ar : $O_2$ from 18 : 2 to 19.8 : 0.2 in standard cc per minute (sccm) during the channel deposition.

For the ozone annealed TFTs, annealing at ≤ 250°C produced good TFTs, while those annealed at 300°C caused large hysteresis and S slope. After applying a high $V_{GS}$ larger than 40 V, the transfer characteristics showed the large $V_{th}$ of 40V and the small hysteresis. Trap state around Fermi level of

the large S state and the large $V_{th}$ state were ~$4x10^{17}$ and ~$1x10^{17}$ $cm^{-3}eV^{-1}$, which were estimated by C-V analysis. The large $V_{th}$ state is very stable in the dark, but the TFT recovers to the initial large S state by light illumination. The photoresponse measurements revealed that deep trap states were formed at 2.3 eV below the conduction band minimum by applying a high $V_{GS}$. Thermal desorption spectra showed that weakly-bonded excess oxygens were incorporated in the a-IGZO layer. From these results, we built a subgap DOS model of the trap states of the excess oxygens. We also confirmed similar behaviors in a-IGZO TFTs fabricated in high oxygen pressure conditions.

This study reveals that the control of oxygen stoichiometry is important for obtaining good performance and stability of AOS TFTs.

5:00pm **TC+EM+NS-ThA10 Effects of Low-Temperature Annealing and Deep Traps in Operation Characteristics of Amorphous In-Ga-Zn-O Thin-Film Transistors**, ***T. Kamiya***, *Y. Kikuchi, K. Ide, K. Nomura, H. Hosono*, Tokyo Institute of Technology, Japan

Amorphous oxide semiconductors (AOSs) represented by a-In-Ga-Zn-O (a-IGZO) are expected for channel materials in thin-film transistors (TFTs) for next-generation flat-panel displays such as jumbo-size / fast / ultrahigh-resolution liquid-crystal displays and organic light-emitting diode displays. These are also expected for flexible electronics devices because they may be fabricated on unheated substrates, and thus produce flexible displays and circuits on inexpensive plastic substrates such as PET. On the other hand, it is known that, although room-temperature fabrication is possible for AOS TFTs, post-deposition thermal annealing at ≥300°C is better employed to obtain good stability. To employ this technology to the flexible electronics, the annealing temperature should be lowered to 200°C or far below. We reported that wet $O_2$ annealing produces the best performance TFTs when annealed at ≥300°C, while it caused serious negative threshold voltage ($V_{th}$) shift at ≤200C. In this paper, we report the origin of the negative $V_{th}$ shift by employing photoresponse spectroscopy of TFT characteristics. It revealed that the near-valence band maximum (VBM) states are reduced significantly even by the low-temperature 200C annealing, and implied that the negative $V_{th}$ shift originates from free electrons released by annihilation of the near-VBM states.

5:20pm **TC+EM+NS-ThA11 β-alumina (SBA): A Promising High Dielectric Constant Gate Material for Solution Processed, Transparent and Low Voltage Transistor Devices**, ***B. Zhang***, *Y. Liu, H. Katz*, Johns Hopkins University

β-alumina (SBA) has been discovered as a promising high dielectric constant gate material for solution processed, transparent and low voltage transistor devices. Some experimental evidence indicates that the mobile Na ion within two spinel blocks made by Al and O is responsible for the high dielectric constant. Transistors (W/L ratio 10) using SBA as gate layer and zinc tin oxide (ZTO) as active layer only need 2V to obtain 0.7mA output current. SBA material is compatible with organic semiconductors such as PQT12 and pentacene as well. Some key issues regarding using SBA for real applications, such as device stability in the ambient atmosphere, response under high frequency, and threshold voltage shift under gate bias have also been studied. It is found that encapsulating the device with CYTOP fluorinated polymer is an effective way to increase the operational stability of the devices in the ambient environment.

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