Plasma Science and Technology Division
Room: 201 - Session PS-TuM

Advanced BEOL / Interconnect Etching I

Moderator: A. Balakrishna, Applied Materials, Inc.

8:00am **PS-TuM1 Narrow Pitch Dual Damascene Patterning using EUV Lithography in Association with a Spin-On Trilayer Resist System**, ***F. Lazzarino***, *V. Truffert, B. Vereecke, S. Demuynck*, IMEC, Belgium

Extreme ultraviolet lithography (EUVL) is one of the leading candidates for the 22-nm node device manufacturing. However, a major issue is the necessity to use thin photoresist (between 55-nm and 80-nm after development) because of resolution requirement and limited depth of focus. In addition, its low etch resistance does not allow high aspect ratio pattern transfer. In this context, a new hardmask strategy called spin-on trilayer resist system has been considered.

In this work, we mainly focus on the etch patterning capability of narrow pitch dual damascene structures by using EUVL combined with a spin-on trilayer resist system. The latter consists of three layers. The photoresist on top is used to pattern a thin spin-on glass layer which is then used to pattern a thick spin-on carbon layer (SOC). The SOC has two functions. It is used for its good gap-filling capability to avoid patterning over nonplanar surfaces but it also acts as a hardmask to pattern the dielectric stack (150-nm of oxide on top of 15-nm of SiCO and 5-nm of SiCN). Regarding the dual damascene architecture, two different approaches have been considered: the via-first and the trench-first. Despite few challenges such as the well-known fencing issue, the via-first approach has been chosen as it is less sensitive to misalignment. In this scheme, two lithography and etch steps are needed, first to form the via then to pattern the trench and etch the barrier layer. In this study, we compared the via opening by using the standard PECVD carbon layer and by using the SOC layer. As expected, the PECVD carbon layer has a better process window compared to the SOC layer. The selectivity is greater and allows many chemistry variations to fine tune for instance the profile. To get similar process window with the trilayer resist system, we introduced C4F8 and CO to substitute C4F6 and O2 in the original chemistry. This modification clearly improved the process by having a better control on the passivation layer formation. Regarding the trench opening, we observed a significant line wiggling of the SOC hardmask for 50-nm half-pitch structures and beyond. We characterized this instability thanks to stress measurements and we kept it under control by changing three different process parameters: the bottom electrode temperature, the baking conditions after coating and the film thickness. Each of them has an impact but the best result came from combining all three together.

To conclude, we demonstrated that narrow pitch dual damascene structures can be obtained by using EUVL in association with a spin-on trilayer resist system. The structures formed in this way shows good electrical characteristics.

8:20am **PS-TuM2 TiN Hard Mask Integration Line Wiggling Onset: Etching Time Dependence**, ***G.A. Delgadino***, Lam Research Corp.

Cu resistivity increase at smaller geometries and the use of lower κ dielectrics forced several changes on BEOL integration. Susceptibility of ULK material to strip damage drove the adoption of TiN hard mask integration starting with a few players at 65nm node to full adoption at 32nm for advance logic.

TiN hard mask demonstrated good selectivity during dielectric etch but concerns arise as we move to smaller pitch: 1- TixFy residues may compromise metallization of small features and 2- Residual compressive stress in the TiN may induce line wiggling. This last concern is the focus of this work.

We develop a simple analytical model based on Energy balance to predict wiggling onset based on geometrical and mechanical properties of the materials. We showed that the wiggling onset aspect ratio reduces with the pitch. We also shown that even when at the end of the process the no-wiggling condition is satisfied, wiggling might have occurred during etch causing feature distortions.

8:40am **PS-TuM3 Surface Reaction Control for BEOL Application**, ***M. Fukasawa***, *T. Tatsumi*, Sony Corporation, Japan **INVITED**

Increasingly there are more challenges of controlling the plasma processes for BEOL integration, which include the Cu/low-k interconnects, contact hole etching, etc. The presentation will give an overview of the surface reaction control during plasma processes. The main focus is damage reduction and suppression of process fluctuations.

Reducing the damage to low-k dielectrics caused by plasma exposure is one of the key issues. O_2-based plasma has been widely used for ashing the photoresist on low-k SiOCH. H_2-based plasma is employed for the etching of organic low-k film as well as the ashing of photoresist. The origin of damage generation is classified by ions, radicals, and UV/VUV radiation. It was found that not only the ions but also the synergy of radicals and UV/VUV radiation cause a significant amount of damage in the SiOCH, measured by using the pallet for plasma evaluation (PAPE).[1] Hence, precise control of incident ions, radicals, and UV/VUV radiation is required for controlling the surface reactions.

In addition to the precise control of incident species, the optimization of subsequent processes (wet treatment, annealing, etc.) are very important to obtain sufficient electrical yields and reliabilities. The remaining damaged layer after wet treatment degrades the Cu and SiOCH surface and corrupts the interface between the Cu and barrier metal. For instance, the desorbed H_2O from the SiOCH damaged layer causes the oxidation of barrier metal, which results in a shorter EM lifetime. The surface modification during SiCN and SiN etching by CH_xF_y-based plasma and its impact on the electrical yields will also be discussed.

The suppression of fluctuation is also required in the advanced interconnects. Although statistical prediction is one of the approaches to realize stable processes, there is a limitation of prediction accuracy for purely statistical predictions due to the lack of physical models. Thus, the combination of statistical and physical models for highly accurate prediction has become an emerging trend in mass production. We will demonstrate a novel statistical etch rate prediction model by considering the fluctuation caused by the plasma-wall interactions.[2]

The developed prediction model is one of the approaches to realize stable processes. Changes in the spatial distribution of reactive species in the etching chamber are, however, very difficult to detect in current mass production tools. Thus, greater progress of the *in-situ* monitoring tools and prediction methods based on the physical model (simulation) are strongly required in the near future.

1. S. Uchida et al., JAP 103, 073303 (2008).

2. M. Fukasawa et al., JJAP 48, 08HC01 (2009).

9:20am **PS-TuM5 Trench First Metal Hard Mask RIE for the 22 nm Node and Beyond**, ***Y. Feurprier***, *R. Gaylord, Y. Chiba, K. Kumar, D. Trickett,* TEL Technology Center, America, LLC, *Y. Mignot,* ST Microelectronics, *R. Srivastava, T. Kwon, R. Koshy, C. Labelle,* GlobalFoundries, *Y.J. Park,* Samsung, *E. Wormyo, S. Allen,* IBM Research, *E. Soda,* Renesas Electronics, *D. Horak, Y. Yin, J. Arnold,* IBM Research, *M. Ishikawa, H. Tomizawa*, Toshiba America Electronic Components

Trench First metal Hard Mask (TFmHM) integration scheme for BEOL has gained traction over recent years because it can mitigate many challenges that are inherent with Via First Trench Last (VFTL) scheme. This integration scheme was more recently shown to enable Self-Aligned Via (SAV) patterning. The SAV patterning implies a pretty drastic change of the via process as, on top of the usual via requirements, the via patterning process needs to be selective to the metal HM. Key process parameters including temperature, gas chemistry, power and pressure were investigated. The required selectivity of the materials and tight CD control capability necessitate temperature controllable chucks eventually allowing greater process flexibility for both via and trench patterning.

The simultaneous control of via, trench and chamfer profiles (i.e. Critical Dimensions, depth, taper profile, etc), implies the need for better control of the metal HM selectivity during both SAV and trench patterning and the need for flexible adjustment of the ion energy and control of the flux of ions and active neutrals. Low-k material damage control is always pertinent in the RIE process as dimensions get smaller. As the direct result of such tight process guidelines, the hardware challenges arise and new dimensions in process controls are needed.

In this paper, the RIE efforts on process controls of the via and trench profiles, the metal HM selectivity, associated hardware solutions and future process flow options under TFmHM scheme will be discussed.

This work was performed by the Research and Development team at TEL Technology Center America in joint development with IBM Research Alliance Teams in Albany, NY 12203. This work has also been supported by the independent Bulk CMOS and SOI technology development projects at the IBM Microelectronics Div. Semiconductor Research & Development Center, Hopewell Junction, NY 12533.

9:40am **PS-TuM6 Plasma Processing of Ti and TiN Metal Hardmasks for Dielectric Etch**, ***F. Weilnboeck****, *E. Bartis, S. Shachar, G.S. Oehrlein,* University of Maryland, College Park, *D. Farber, T. Lii, C. Lenox*, Texas Instruments Incorporated

Ti and TiN metal hardmasks are of interest for plasma-based pattern transfer into low-k materials due to their expected improvements of etch performance and process flow relative to resist masks. We have studied the performance of Ti and TiN in CF_4/Ar and C_4F_8/Ar discharges along with organosilicate glass (OSG) - a reference low-k material. Plasma processes were characterized in real-time by in-situ ellipsometry and provided information on erosion stages, etch rates (ER) and selectivity (SEL), i.e. ER(OSG)/ER(hardmask). Post plasma characterization was performed by vacuum transfer x-ray photoelectron spectroscopy (XPS). Plasma parameters investigated were: 1) ion energy, 2) pressure, 3) Ar dilution, 4) O_2 addition and 5) N_2 addition to fluorocarbon/Ar mixtures. Furthermore, we have studied chamber wall contamination and surface reactions upon atmospheric exposure of processed Ti/TiN hardmasks. Ellipsometric multilayer modeling of real-time measurements showed three hardmask erosion stages: 1) initial removal of surface oxides, 2) steady state erosion with F-saturated hardmask surfaces (TiFx, x~3) covered with a FC film (0.8-1.6nm depending on plasma conditions) and 3) small amounts of Ti remaining on the underlayer after erosion of the hardmask layer. For all plasma conditions, Ti provides systematically lower ERs and higher SELs (~15) than TiN (~11). The higher ERs of Ti over TiN can be explained by the rapid removal of N by formation of NF_3 and the smaller Ti-atom number density of TiN compared to Ti. Surprisingly, the more polymerizing C_4F_8 conditions lead to lower SELs than CF_4. This observation is explained by FC layer-induced OSG ER reduction, whereas for the hardmasks materials ER are limited by product volatility and the FC surface layer effect is reduced, e.g. as compared to conventional organic masking layers. Chamber contamination studies have shown that only small amounts of Ti (<1%) are deposited together with FC on the chamber wall. Overall, metal hardmasks, especially Ti, showed excellent performance as a masking material in low-k etch and provide high SEL (~15) which can be further increased by systematically optimizing discussed plasma parameters.

11:00am **PS-TuM10 Superposition of High Negative DC Voltage in Capacitively Coupled Plasma**, *A. Ranjan,* ***A. Metz****, A. Lisi, Y. Chiba, W. Li, Y. Feurprier, K. Kumar, P. Biolsi,* TEL Technology Center, America, LLC, *L. Chen, P. Ventzek, R. Sundararajan*, Tokyo Electron America

The effects of applying a negative DC voltage to capacitively coupled plasmas (CCP) were investigated using PIC-MCC simulation and experiment. High energy secondary electrons, originating at the electrode with high negative DC voltages (DC electrode), are generated due to ion impact as well as electron-impact. These secondary electrons are accelerated away from the DC electrode by the sheath voltage drop. These secondary electrons gain energy equal to DC voltage drop across the sheath and travel to wafer electrode or get trapped between electrodes. Trapping and dumping of ballistic electrons depends on the voltages on the electrodes. Ballistic electrons alter the bulk electron energy distribution function of the plasma (EEDF), EEDF at wafer, high energy electron flux to wafer and plasma density profiles. Simulation shows that center to edge uniformity, plasma density and EEDF can be tuned by applying negative DC voltage in CCPs. Bulk plasma volume can be modulated by applying negative DC voltage giving us a very effective knob for an "effective" variable gap CCP without moving chamber parts in vacuum. The change in EEDF alters the plasma chemistry, the result of which can be observed by optical emission spectra and blanket etch rate data, validating the changes in chemistry due to superimposed negative DC voltage. Various other interesting aspects will also be presented.

11:20am **PS-TuM11 Evaluation of C5HF7: A High Etch Selectivity Hydrogen-Containing Fluorocarbon Gas for Oxide Etch**, ***R.L. Bruce***, IBM T.J. Watson Research Center, *M. Nakamura,* ZEON Chemicals L.P., *S. Engelmann, E.A. Joseph,* IBM T.J. Watson Research Center, *G. Matsuura,* ZEON Chemicals L.P., *N.C.M. Fuller, E.M. Sikorski, W.S. Graham, Y. Zhang,* IBM T.J. Watson Research Center, *A. Itou*, Zeon Corporation

A high etch selectivity hydrogen-containing fluorocarbon gas, C5HF7, was evaluated for high aspect ratio dielectric etch. Plasma etching with Ar/C5HF7/O2 chemistry was shown to have significant advantages over Ar/C4F6/O2 in terms of oxide-to-organic mask etch selectivity and line-edge roughness. The mechanism behind the high etch selectivity of C5HF7 originated from the different thickness and composition of steady-state fluorocarbon (FC) layers generated on oxide and organic mask materials during plasma etch. We also determined that hydrogen addition to the Ar/C4F6/O2 feedgas did not reproduce C5HF7 etch behavior, presumably due to the difference in atomic hydrogen formation between molecular H2 dissociation versus intramolecular H dissociation (from C5HF7). This latter phenomenon facilitated a wider window for "etch stop" margin. Profile evaluation showed larger bowing for C5HF7, compared to C4F6, and was linked to a higher sticking coefficient of CxFyHz radicals. This was verified and remedied by increasing the substrate temperature, which reduced the radical sticking coefficient and eliminated bowing, while maintaining the high etch selectivity. We also demonstrated reduced low-frequency line-edge roughness when etching with C5HF7. We showed that less surface roughness was generated using C5HF7 since less organic mask thickness was removed. In addition, since a major contribution of line-edge roughness was the transfer of organic mask surface roughness into the sidewalls of the dielectric, overall lower line-edge roughness was observed.

11:40am **PS-TuM12 Etch Uniformity Improvement Using Mid-Gap Capacitively Coupled Plasma**, ***C. Cole****, A. Ko, A. Ranjan, T. Enomoto, A. Metz, K. Kumar, P. Biolsi,* TEL Technology Center, America, LLC, *E. Wornyo, H. Yusuff, S. Allen, R. Wise,* IBM Research, *C. Labelle, T. Chen,* GlobalFoundries, *S. Kanakasabapathy,* IBM Research, *Y. Mignot*, STMicroelectronics

As device dimensions continue to shrink, uniformity of etch rate/feature depth and critical dimension becomes very important. Capacitively coupled plasma (CCP) sources have advantage in terms of uniformity over non-planar sources in addition to design simplicity, reliability and wide process window. Wide-gap CCPs have been used for front-end etch applications where as small-gap CCPs are work-horse for back-end dielectric etch. Recently, studies on mid-gap CCPs indicates that inter-electrode spacing of ~100mm is best suited for etch rate and CD uniformity. In our studies, for tri-layer mask etch and TiN hard-mask etch, mid-gap CCP achieved uniformity of <1nm (3σ) CD and ~1% (3σ) etch rate. Mid-gap CCPs have 20-30% higher etch rate compared to wide-gap CCPs. Power on top electrode can be divided to center and edge for control of plasma density distribution. Design changes in pumping port assembly effectively create uniform confined plasma without plasma leaking through pump-port. Plasma confinement helps in creating denser plasma at relatively lower RF power. Using above-mentioned "knobs", flat etch rates and CDs were achieved in mid-gap CCPs.

This work was performed by the Research and Development team at TEL Technology Center America in joint development with IBM Research Alliance Teams in Albany, NY 12222. This work has also been supported by the independent Bulk CMOS and SOI technology development projects at the IBM Microelectronics Div. Semiconductor Research & Development Center, Hopewell Junction, NY 12533.

***** Coburn & Winters Student Award Finalist

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