Plasma Science and Technology Division
Room: 201 - Session PS-MoM

Advanced FEOL / Gate Etching I

Moderator: A. Agarwal, Applied Materials, Inc.

8:20am **PS-MoM1 Impact of Synchronized Plasma Pulsing Technologies on Key Parameters Governing STI Etch Processes**, ***M. Haass****, *M. Darnon*, *G. Cunge*, *P. Bodart*, *C. Petit-Etienne*, *M. Brihoum*, *L. Vallier*, LTM-CNRS, France, *S. Banna*, Applied Materials, Inc., *O. Joubert*, LTM-CNRS, France

Plasma etch processes are the only technological solution to address the critical dimension control at the nanometer range imposed by the continuous downscaling of CMOS device dimensions in microelectronics. However, the current processes are reaching their limits of controlling etch selectivity, defects, critical dimensions and uniformity. Lately, pulsed plasmas are increasingly used to overcome some of these limitations. On the basis of HBr/O_2 plasmas, dedicated to STI (Shallow Trench Isolation) etching, we discuss the role of the pulse parameters regarding the etched profiles, the reactive etch layer, the uniformity and the passivation layer. To investigate the passivation layer at various trench depths and CDs we developed a new XPS technique for quasi in-situ chemical topography analysis.

The experiments are carried out in a 300 mm AdvantEdge™ tool from Applied Materials Inc. The two generators to sustain the plasma (ICP) and to polarize the wafer (CCP), operated at 13.56 MHz, have been modified with the Pulsync™ system to allow pulsing at a wide range of parameters. However, only synchronous pulsing is studied here. Moreover, a Theta300 angle resolved XPS system from Thermo VG is connected under vacuum, allowing quasi in-situ analysis of an etched sample. Several additional diagnostic methods including time resolved UV-absorption, mass spectroscopy and ellipsometry are used to study the impact of pulsing the plasma on the surface and the gas phase compared to a continuous wave process.

We demonstrate that plasma pulsing can minimize the mask faceting and consumption which is due to a change in the ion energy distribution and the presence of larger molecular ion species. The duty cycle controls the formation of the passivation layer that governs in turn the form of the etched profiles. This correlation can partly be explained by less dissociated oxygen molecules in low duty cycle pulsing. Nevertheless, XPS analyses show that the chemical composition of the passivation layer changes little with height and trench CD while its thickness is directly linked to the aspect ratio of the analyzed part of the sidewall. Less thickness variation with respect to the aspect ratio is observed in pulsed mode, which explains an improved local uniformity in profile evolution. Furthermore, the time compensated etch rate with respect to the actual ON time of the plasma is increasing at low duty cycles due to a change of etch regime from more radical flux limited to ion flux limited. Nevertheless, the overall process etch rate is decreasing in pulsed mode which can be partly counteracted by increasing the source and the bias power.

8:40am **PS-MoM2 Effect of Si Damage on Shallow Source-Drain (SSD) Recess Structures**, ***J. Guha***, *S. Sriraman*, Lam Research Corporation

Continued scaling in the semiconductor industry provides new challenges for critical Front-end-of the-line (FEOL) process etch applications in front-end logic devices. One such application that is utilized in the PMOS transistor is the Strained Source Drain recess (SSD) structure that embeds an epitaxial strained SiGe thin film that significantly improves hole mobility in the channel region. Scale down of critical dimensions (CD) in current and future CMOS devices puts ever increasing emphasis in reducing post-etch Si surface damage in a source-drain (SD) recess structures. For a typical SSD application, the roughness of Si surface obtained after SD etch governs both the epitaxial growth of SiGe as well as the roughness of the SiGe layer, and ultimately determines the device performance. This paper will discuss the factors that contribute to the Si surface roughness arising from a representative SD process etch step and its impact on the subsequent SiGe epitaxy and device performance. Typically, the SD etch sequence may consist of an anisotropic etch (halogen/oxygen based chemistry) followed by an isotropic etch (halogen/halogen based chemistry). Surface roughness of the etched silicon is quantified and spatially resolved through atomic force microscopy and surface haze measurements, and contributions of the anisotropic and isotropic etch steps to surface roughness are inferred. The effects of halogen ratio and relative halogen atom reactivity in the isotropic etch chemistry on surface roughness and the vertical-to-lateral (V/L) etch ratio in the SSD recess feature will be discussed and a surface reaction model proposed to characterize roughness evolution.

9:00am **PS-MoM3 Improving Etch Processes by using Pulsed Plasmas**, ***M. Darnon***, *M. Haass*, *P. Bodart*, *G. Cunge*, *C. Petit-Etienne*, *M. Brihoum*, *R. Blanc*, CNRS-LTM, France, *T. David*, Cea Leti Minatec Campus, France, *E. Pargon*, *L. Vallier*, *O. Joubert*, CNRS-LTM, France, *S. Banna*, *T. Lill*, Applied Materials, Inc. **INVITED**

The etching processes for integrated circuits fabrication becomes extremely challenging when the devices dimensions are downscaling and the etch process has to stop on the ultra thin layers (less than 2nm) of materials. Perfect control of the passivation layers and mask erosion are required to precisely control the patterns profiles, which necessitates using flows and energies of plasma species in ranges which can not be attainable with current plasma technologies. In addition, limiting the plasma induced damage to thin layers requires very low ion energies which are not accessible in current plasma technologies. One promising solution is to pulse the plasma in conventional industrial reactors at very low duty cycle. Using this solution, the ratio of radicals and ions as well as their energy can be fine tuned in ranges that are unreachable otherwise, and very low energy ions are produced which strongly minimizes the damage to the thin layers exposed to the plasma.

Experiments are performed on a 300mm diameter Inductively Coupled Plasma chamber commercialized by Applied Materials (DPSII G5) equipped with the pulsync system to enable plasma pulsing in an industrial reactor.

In this paper, we will show how plasma pulsing can be used to improve uniformity and pattern profiles by better controlling the passivation layer formed on the patterns sidewalls during the etching. In addition, we will demonstrate that the reduction of the average ion energy as well as the use of molecular ions decreases mask erosion, as well as damage to ultrathin etch stop layers. Morphological characterization, surface characterization and plasma diagnostics will be correlated to explain the mechanisms responsible for the process improvement.

9:40am **PS-MoM5 HfO_2 Etching by Pulsed BCl_3/Ar Plasma**, ***P. Bodart***, *C. Petit-Etienne*, *G. Cunge*, *F. Boulard*, *M. Darnon*, *L. Vallier*, *E. Pargon*, CNRS-LTM, France, *S. Banna*, *T. Lill*, Applied Materials, Inc., *O. Joubert*, CNRS-LTM, France

Plasma etching of high-k materials, including HfO_2, has attracted much attention due to the necessity to integrate these materials in MOSFET transistor. After the metal gate patterning process, the high-k dielectric film must be removed from the source and drain regions of the transistor. It is today well established that HfO_2 can be etched selectively towards SiO_2 and Si in BCl_3/Cl_2 plasma. However, it remains difficult to minimize the plasma induced damages (Si amorphisation and recess) in the source/drain transistor regions in such processes. Since pulsed plasmas have shown a capability to minimize Si-recess in typical silicon gate oxide etching processes, we have investigated their potential for HfO_2 etching.

The experiments are performed in a 300mm DPS tool from Applied Materials. The chamber is modified to allow plasma diagnostic like UV-broad band absorption spectroscopy. The reactor is also connected to an Angle-Resolved X Ray Photoelectron Spectroscopy analyzer by a robotized vacuum chamber. The etching rate of HfO_2 sample (either 40 or 3.5nm-thick HfO_2 films with 8 Å SiO_2 interlayer deposited on Si substrates) and of SiO_2 samples (10 nm thick) are measured in real time by in situ multi-wavelength ellipsométrie.

We have evaluated the capability of pulsed plasmas to minimize the plasma induced damage of silicon during the etching of HfO_2 high-k gate dielectric. XPS analyses show that the perturbation of the bulk Si lattice is less pronounced with pulsed conditions, which is attributed to a lower ion bombarding energy. However, the formation of a BCl_x polymer selectively on the silicon (which is responsible for the HfO_2 to Si etching selectivity) is reduced when the plasma is pulsed leading to a loss of selectivity. VUV absorption spectroscopy indicates that the fragmentation of BCl_3 molecules, which leads to the formation of B-rich polymer precursors, decreases dramatically when the plasma is pulsed at low duty cycle. Therefore, as the duty cycle is reduced, the fluxes of B radicals to the wafer are reduced while the amount of Cl in the polymer increases. It follows that the polymer deposition rate drops, eventually leading to a loss of selectivity at the lowest duty cycles.

However, there are several ways to retrieve the process selectivity in pulsed plasma, such as reducing the BCl_3 flow in the gas mixture or working at higher pulsing frequencies (up to 10 kHz) to enhance B formation in the gas

***** Coburn & Winters Student Award Finalist

phase. Pulsing the plasma is not a magic knob since it strongly changes the range of allows news physics and chemistry ranges plasma parameters.

However, plasma pulsing reduces significantly the plasma induced damages after process optimization.

10:00am **PS-MoM6 Study of Metallic Interfaces Etching for High-K Metal Gate stacks in CMOS 28 nm Technology**, ***F. Chave***, STMicroelectronics, France, *L. Vallier*, CNRS-LTM, France, *P. Gouraud, C. Vérove*, STMicroelectronics, France, *O. Joubert*, CNRS-LTM, France

In CMOS technology, the downscaling of the transistor gate dimension, driven by ITRS roadmap specifications for advanced technology, requires the introduction of new materials. Dry etching step of those new "High-K Metal Gate" (HKMG) stacks is critical for the electrical performances of the devices and needs very accurate process control to achieve correct profiles, with a good Critical Dimension control. Moreover, characterization tools are now dealing with thin materials thicknesses sometimes around the limit of one full atomic layer. In this work we focus on dry etching process of 28nm technology High-K Metal Gate stacks. Several issues, especially for Metal/Capping layer interfaces, are investigated to better understand and control physicochemical interactions.

Most of etching experiments are carried out in a 300mm DPS AdvantageEdge^{TM} etch chamber from Applied Materials allowing in situ diagnostic, as reflectometry and spectroscopic ellipsometry. This modified tool permits to transfer wafer under vacuum to a customized Theta 300 XPS system from Thermo Fisher Scientific for quasi in-situ analysis without exposure to the environment. Samples were 300mm diameter Si wafer with full sheet and/or patterned deposited layers. Industrial 28nm photolithography & plasma etching process developed to gate first approach were employed.

Preliminary experiments have shown that foot and undercut effects are possible profiles deformations due to metallic interfaces, and we have to control these deviations.

Consequently, we focused first on the TiN/LaO interfaces which we highlight as a critical step. TEM analyses demonstrate that LaO capping layer acts as etch stop layer for current TiN etching chemistries. Therefore, a specific step for LaO removal is needed; otherwise etching residues are left over.

Layer thickness and step time in the specific removal of Lanthanum oxide are some parameters which directly impact the under-layer materials with the observation of pitting on nMOS open areas or residues on pMOS.

XPS characterizations were carried out. Etching results analyses for TiN/LaO/TiN interface reveal the fact that after the whole stack etching step, some LaO residues remain on the sample surface although TiN disappear as evidenced from XPS survey scan. The conclusion is that TiN looks totally removed as Lanthanum can be redeposit or for certain push-forward. Such as mechanisms were considered, and experiments were carried out to understand and complete this result.

Integration of thin metallic and capping layers in gate stacks challenge dry etching process. Those results highlight the trend of interactions all across the plasma etch process.

11:00am **PS-MoM9 Double Patterning Challenges for the sub 22nm CMOS Nodes**, ***S. Kanakasabapathy***, *R. Jung, M. Hartig, S. Schmitz, Y. Yin*, IBM Research, *S. Raghunathan, L. Jang*, GlobalFoundries, *E. McLellan, S. Burns, S. Holmes, C.S. Koay*, IBM Research, *R.H. Kim*, GlobalFoundries, *G. Landie*, ST Microelectronics, *D. Horak*, IBM Research, *Y. Mignot*, ST Microelectronics, *S. Seo, S.T. Chen, J. Arnold, M. Colburn, B. Haran*, IBM Research

Wavelength and Numerical Aperture scaling in optical lithography have allowed CMOS density scaling to march along the Moore 's Law curve for the past three decades. However, at the sub 22nm CMOS nodes, the print pitch faces a technological barrier at the 80nm mark for the Front, Middle and Back Ends of Line. Until further wavelength scaling becomes available through Extreme Ultraviolet (EUV), the industry's attention is focused on Double Patterning. Multiple Interdigitated Lithography and Sidewall Image Transfer (SIT) are the two broad categories of techniques under consideration. Interdigitated Lithography can be subdivided into approaches with and without multiple passes through etch. Both of these techniques present unique etch challenges in assembling looser pitch patterns into a composite mask and subsequent pattern transfer into the stacks of interest. We will review etch perspectives on the applicability of double patterning methods to various levels in the process flow.

In particular, Fins for FinFET technology represent the tightest pitch (approximately 40nm for the technology nodes in development at this time) and yield well to Sidewall Image Transfer. We will present the issues surrounding mandrel definition and spacer film properties for Fin definition. The Gate level poses competing requirements of overlay control between the simpler patterns and the need to attain multiple Critical Dimensions (CDs) and pitches. We will examine this and the challenges of etch into advanced gate stacks for the 14nm node. At the Interconnect levels, we will consider the challenges of transferring not only trenches but also self aligned via patterns at sub -40nm half pitch into ultra low-k (ULK) dielectrics.

11:20am **PS-MoM10 Novel Etch Mechanism for High Selectivity Etching of Silicon Nitride over Silicon and Silicon Oxide for Spacer Applications**, ***S. Engelmann***, *J. Chang, E.A. Joseph, R.L. Bruce, N.C.M. Fuller, W.S. Graham, E.M. Sikorski, S. Balakrishnan, A. Banik, M. Gordon*, IBM T.J. Watson Research Center, *M. Nakamura, G. Matsuura*, ZEON Chemicals L.P., *H. Matsumoto, A. Itou*, Zeon Corporation

To continue scaling CMOS devices at the traditional pace following Moore's law, high selectivity of etch processes towards multiple materials is approaching nanoscopic dimensions. The spacer etch process is a very critical element in the CMOS device process flow as it ensures and enables the electrical isolation of source/drain and gate regions. Extremely high precision is needed to form a silicon nitride (SiN) spacer without damaging exposed Si, SiO_2, or other surfaces (SiGe or SiC for example). This process is even more challenging for non-planar devices (such as FinFETs and Trigates), where the plasma process needs to be able to form the spacer on the gate sidewall, but not the fin sidewall. At the same time the exposed SiO_2 and Si surfaces (if applicable) have to withstand the extended processing necessary to form the spacer.

Multiple etch gas chemistries have been evaluated and their impact on etch rates and selectivities for spacer applications have been evaluated. Surface analysis techniques such as XPS and FTIR have been applied in conjunction with OES analysis of the plasma to study the etch mechanisms leading to the observed etch rates. Fundamental differences in etch mechanism were found for different etch gas chemistries.

We observed that during conventional spacer processes, very little difference in plasma polymer deposition onto the respective substrates could be noted. A successful SiN spacer process was rather facilitated by a Si etch process that was selective to SiO_2, where excess oxidation lead to a conversion of Si to SiO_2. This also means that the etch rates of the SiN are limited by the simultaneous oxidation of the same. A potential solution to overcome this limitation would be to control the etch rate by polymer thickness, similar to high selectivity SiO_2 etching. An evaluation of this approach has yielded similar results as the general etch mechanism proposed by Schaepkens et al.[1] [#_ftn1] A novel etch chemistry was also evaluated that enables a different etch mechanism that cannot be described by the general model. The impact of the described mechanisms on actual CMOS devices will be discussed in detail.

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[1] [#_ftnref1] M. Schaepkens et al., J. Vac. Sci. Technol. A 17, 26 (1999)

11:40am **PS-MoM11 High-Aspect Silicon Trench Oxidation in Downstream of Surface-wave Oxygen Plasma**, *Y. Taniuchi*, ***H. Shindo***, Tokai University, Japan

A low temperature and low damage silicon oxidation technique is highly required in various technology fields, such as in ULSI insulation layer formations, MEMS (Micro-Electro-Mechanical System) processes and other material surface treatments. In particular, in ULSI, the shallow trench isolation (STI) technique is inevitable to realize further integrations. In this process, so-called, a liner oxidation, in which the trench bottom is directly oxidized, becomes more severe, as the trench aspect ratio is further increased with the integrations. In MEMS (Micro-Electro-Mechanical System) processes, on the other hand, deep silicon trench etching with high aspect ratios is one of key technologies, and to realize a deep trench etching with a good directionality, a side wall passivation by the trench oxidation is inevitable. In this work, a silicon trench oxidation is investigated by employing a microwave oxygen plasma downstream under the condition of radio-frequency bias as well as the DC. In particular, the radio-frequency bias and the DC are superimposed and applied onto the substrate with the trench structure, and the oxidation rates at various portions of trench with the aspect ratio of 2 to 6 are examined as a function of the superimposed substrate bias. The oxidation depth shows a maximum in a very downstream of further position from the microwave window, indicating that the oxidation is due to negative oxygen ions. The silicon trench oxidation mapping, in which the oxidation film thickness is two-dimensionally plotted for the radio frequency bias and DC bias voltages, clearly demonstrates that the maximum is brought about along the line of the substrate bias of +20 V just above the plasma potential. In particular, the silicon trench bottom oxidation is just limited onto the higher radio frequency bias within the above condition. As for the dependence on the trench aspect ratio R, the oxidation at the trench bottom was attained 100 % of the trench top up to R=3, while at the trench bottom with R more than 4 it was only 60 %. The oxidation at the bottom of deep trench with the aspect ratio R= 6 was

improved at the higher radio frequency bias. It is concluded that the oxidation is due to the negative oxygen ions in downstream.

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