Tuesday Morning, November 1, 2011

Plasma Science and Technology Division
Room: 202 - Session PS+MN+TF-TuM

Plasma Processing for Disruptive Technologies
Moderator: M.C.M. van de Sanden, Eindhoven University of Technology

8:00am **PS+MN+TF-TuM1 Scallop Free TSV Etching Method for 3-D LSI Integration**, ***Y. Morikawa***, *T. Murayama, T. Sakuishi, S. Toyoda, K. Suu*, ULVAC, Inc., Japan **INVITED**

Thru silicon via (TSV) etch process for deep and high-aspect ratio structure has been studied thoroughly for applications such as MEMS and CMOS devices. Recently, TSV used in 3D-LSI devices for logic devices may be a few microns in diameter and about 50 um deep. On the other hand, TSVs used in stacking memory devices, the via diameter and depth would be several tens of microns. Therefore, development of TSV etching process is very important for realizing these applications. In this study, a large via size etching in a high-pressure process was focused by using very high frequency capacitive coupled plasma (VHF –CCP) with an ultra self-confined system. This plasma system is simple parallel plate CCP about 100Pa or more process. High-pressure process was carried out on the plasma confined, because mean free pass is very short. And, ion energy distribution (IED) is also controllable by high-presser process with VHF bias. The bimodal IED changes under high-pressure. The peak of high-energy side is reduced, and a charge exchange peak appears. It is considered that the charge exchange is important to anisotropic Si etching of large size TSV with VHF bias.

And next, the high-density and small size of TSV below 10um diameter is indispensable to the utilization and improvement in high performance of 3D-LSI. We have developed a new etching system for TSV application for small size and high aspect ratio via. This system is a planer type magnetic neutral loop discharge (NLD) plasma. For high rate silicon etching, it is very important to understand not only the high density of the ICP plasma generation but also the high density of fluorine atoms. In this study, a novel RF antenna 'Multi Stacked rf Antenna' has been developed for highly accurate and high rate etching process. This antenna consists of multistage spiral turn rf antennas to reduce self-inductance (L). The L of this antenna is below 1.0 uH and it is a lower than the standard spiral antenna. As a result of performing the electron density measurement of the planer NLD plasma using this MS antenna, it succeeded in the high-density plasma production of $1x10^{12}$ / cm^3 by the process pressure of 7 Pa. Next, the Si etching process development was performed using the advanced NLD etcher. As a result, the etching rate improved 4 times more compared to the standard cylindrical NLD plasma. Finally, the diameter of 2um was attained by the anisotropic etching of 5 um/min, and the aspect ratio is above 10 using the planer NLD etcher. VHF CCP and planer NLD etching processes are non-cycle etch methods, and these processes were demonstrated about smooth sidewall TSV formation.

8:40am **PS+MN+TF-TuM3 Deep Silicon Etching of 0.8 µm to Hundreds of Microns Wide Trenches with the STiGer Process**, ***T. Tillocher***, *W. Kafrouni,* GREMI, France, *J. Ladroue,* STMicroelectronics - GREMI, France, *P. Lefaucheux,* GREMI, France, *M. Boufnichel,* STMicroelectronics, France, *P. Ranson, R. Dussart*, GREMI, France

The STiGer process is designed to achieve high aspect ratio features in silicon. Like the Bosch process, passivation steps (SiF4/O2 plasmas) and etching steps are cycled to get vertical structures. The etching steps can be purely isotropic (SF6 plasmas) or anisotropic (SF6/O2 plasmas). It is required to cool the silicon substrate with liquid nitrogen to form a SiOxFy passivation layer. It desorbs and disappears when the substrate is heated back to room temperature. Thus, there is no need to clean neither the microstructures nor the chamber walls after each process run. Then, the robustness of the process is enhanced in comparison with standard cryoetching: the profiles are less sensitive to temperature or flow rate variations. But, like in Bosch etching, a scalloping is present on the sidewalls.

Submicron trenches having critical aperture of about 0.8 µm can be etched with high aspect ratios (> 40). In these cases, the average etch rate is around 1.8 µm/min. These features exhibit both undercut and a special defect, which is called "extended scalloping". This defect is composed of anisotropic cavities developed on the feature sidewalls, just below the mask. It originates from ions scattered at the feature entrance that hit the top profile and remove locally the passivation layer. This defect is observed only for high aspect ratios (typically above 10). Thus, we will also investigate the role of trench critical dimension (from 0.8 µm to 100 µm). A mechanism explaining the formation of the extended scalloping will be proposed.

We have studied the influence of both the duty cycle (tetch/(tetch+tpassivation)) and the chamber pressure on the profiles and the extended scalloping. Basically, when the duty cycle increases, etching dominates passivation, which leads to higher defects. Pressure is a way to tune the slope of the sidewalls. Actually, decreasing the chamber pressure helps to shift from positively tapered features to more vertical profiles, and even negative slopes, hence with dovetailed shape.

This will be correlated with plasma analysis by means of mass spectrometry and optical emission spectroscopy. Actually, it is relevant to investigate how changes in the plasma chemistry can modify the trench profiles.

These trends have been used to optimize two methods that can help to reduce the extended scalloping. The first consists in adding a low oxygen flow in the etch cycle, favouring a low additional passivation. The second technique consists in gradually increasing the SF6 flow from a low value to the nominal value. Consequently, the process starts with a low etch rate and a more efficient passivation, which helps to limit the extended scalloping.

9:00am **PS+MN+TF-TuM4 Evaluation of Alternative Passivation Chemistries for TSV Applications**, *E.A. Joseph,* IBM T.J. Watson Research Center, *G. Matsuura,* ZEON Chemicals L.P., *S. Engelmann,* IBM T.J. Watson Research Center, *M. Nakamura,* ZEON Chemicals L.P., ***N.C.M. Fuller***, *E.M. Sikorski, M. Gordon, B.N. To,* IBM T.J. Watson Research Center, *H. Matsumoto, A. Itou*, Zeon Corporation

With the current advent of 3D integration for advanced interconnect and packaging applications, there has been a renewed focus on deep silicon etch technology to satisfy the need for Through Silicon Via (TSV) patterning. The most common etch method used to fabricate said devices is a time-muliplexed (BoschTM) process, based on years of maturity in the MEMS field.[i] However, issues such as scalloping, mask undercut and limited etch rates are becoming more pronounced as feature sizes scale to meet the ITRS roadmap requirements. This has prompted efforts to attempt to either develop a more conventional etch process[i][ii]or to modify the Bosch process to circumvent these issues.[iii][iv] [v] In this work, we explore a novel polymerizing feedgas chemistry for the deposition step of the Bosch process to improve mask undercut while simultaneously increasing TSV etch rate. Initial results indicate a 5x larger deposition rate as compared to C4F8 (under nominal conditions) and under optimized conditions, enables a 50% decrease in undercut along with 10% increase in TSV etch rate. Optical emission spectra also differ substantially between the two feed gases, indicating different dissociation pathways and radical densities. Further results and a detailed characterization of the deposition properties of the novel chemistry will also be discussed leading to a proposed mechanism for the profile improvements as compared to C4F8. [i] B. Wu, A. Kumar and S. Pamarthy, J. of Applied Physics 108, 051101 (2010) [ii] I. Sakai, N. Sakurai and T. Ohiwa, J. Vac. Sci. Technol. A 29(2), Mar/Apr 2011 [iii] N. Ranganathan et al, Proceedings of the Electronics Components and Technology Conference, 2005 [iv] H. Rhee et al, J. Vac. Sci. Technol. B 27(1), Jan/Feb 2009 [v] S.-B. Jo et al, J. Vac. Sci. Technol. A 23(4), Jul/Aug 2005

9:20am **PS+MN+TF-TuM5 Wafer Scale Hermetic Packaging of MEMS**, ***C.S. Gudeman***, IMT **INVITED**

The explosion of MEMS in automotive and cell phone markets has been enabled by low cost wafer level packaging (WLP) technology that provides a robust and hermetic enclosure for an otherwise delicate device. The more obvious advantage of WLP is greatly improved reliability, because the device is protected from organic and particulate contaminants while in the hands of the end user. A less obvious advantage is the protection provided by WLP during the manufacturing process, which often produces the highest levels of stress that a MEMS device experiences. These processes include wafer grinding, wafer dicing, and chip solder re-flow attachment to circuit boards and other chips. Firstly in this talk, wafer level packaging technologies will be outlined, focusing on the truly hermetic methods -- alloy, glass frit, Au-Au thermo-compression, anodic, and fusion bonding. Secondly the integration of Through Silicon Vias (TSV) with WLP will be discussed. Finally the performance of these technologies will be compared from a manufacturing perspective, including yield and thermal budget.

10:40am **PS+MN+TF-TuM9 Challenges in Plasma Etch for NVM: Scaling and Materials**, ***M. Kiehlbauch***, Micron Technology, Inc. **INVITED**

With advances in non-volatile memory, the major challenge confronting plasma etch is the introduction of new materials while simultaneously shrinking critical dimensions. This talk will address key development aspects including profile control, feature level uniformity, and plasma microdamage. Plasma microdamage is not the traditional, charge/voltage/current based impact to, for example, gate oxides. Rather, it is the changes to the atomic scale morphology in the sidewall or landing film of a plasma etch process. This results in a disruption of local stoichiometry, film defects, and other issues that impact device performance. The etch process and hardware changes to address this will be presented.

11:40am **PS+MN+TF-TuM12 Mechanisms of Selective Etching for Magnetic Materials: Ni, Co and Ta Etching by Carbon Monoxide/Methyl Alcohol Based Plasmas**, ***K. Karahashi***, *T. Ito*, *S. Hamaguchi*, Osaka University, Japan

Dry etching of magnetic thin films is a crucial step in micro fabrication of magnetic random access memories (MARMs) and read/write heads for magnetic data storages. Argon (Ar) ion milling seems to be almost the only etching technique available in the current manufacturing processes. However Ar ion milling is incapable of achieving anisotropic and selective etching of magnetic films (Ni, Co etc.) over hardmasks (Ta etc.) and therefore highly selective reactive ion etching (RIE) of magnetic thin films is a highly sought-after technology. RIE processes based on CO/NH_3 or CH_3OH is a candidate for selective etching of magnetic thin films. In this study, we have examined etching processes of Ni, Co and Ta thin films by energetic CO^+, O^+ or OH^+ ions, which are considered to be major etchants of CO/NH_3 or CH_3OH plasmas. We have determined the etching yields and analyzed surface reactions, using a mass-selected ion beam system. The ion beam system is designed to inject mono-energetic single-species ions into a sample surface in ultra-high vacuum conditions. The reaction chamber, where the sample is placed, is equipped with an X-ray photoelectron spectroscopy (XPS) for in-situ chemical analyses of irradiated surfaces. The ion beam energy used in this study is in the range of 150-1000 eV. The etching yields are determined from measured depth profiles of irradiated surfaces and ion fluxes. The etching yields of Ni and Co by CO^+ ions are higher than that by O^+ ions but lower than the yields of possible physical sputtering, which are estimated from interpolation of sputtering yield data of inert atom ions (He^+, Ne^+, Ar^+, Kr^+ etc.). From XPS analysis for O^+ irradiated Ni and Co surfaces, oxidation is found to occur under O^+ irradiation, which suggests that the oxide layer hinders sputtering by ion bombardment. It is found that little oxidation occurs on Ni or Co surfaces under CO^+ ion irradiation and etching by CO^+ ion bombardments proceeds. On a Ta surface, on the other hand, in the both cases of O^+ and CO^+ irradiations, oxidation occurs and its etching yield is far smaller than the yield of its possible physical sputtering. Therefore we have found that high selectivity of Ni and Co etching against hard masks (Ta, TaN) arises from the prevention of sputtering by mask oxidation. Etching characteristics by OH^+ irradiation were also studied in a similar manner. This work was supported by the Semiconductor Technology Academic Research Center (STARC).

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