Nanometer-scale Science and Technology Division
Room: 203 - Session NS+EM-MoM

Nanowires and Nanoparticles I: Assembly and Devices

Moderator: M. Hines, Cornell University

8:20am **NS+EM-MoM1 ZnO Nanowire Logic Inverter with the Difference of Two Gate Electrode**, *J.K. Kim*, ***Y.T. Lee***, *R. Ha, H.J. Choi, S.I. Im*, Yonsei University, Republic of Korea

Recently, zinc oxide nanowires (ZnO NWs) have attracted much attention for high mobility and sensing properties. These advantageous give us strong possibility to use nanostructures as nanoelectronic device application; such as field effect transistors (FETs), diodes, and logic circuit devices.[1] In this work, we fabricated the logic circuit inverter using difference of gate electrodes which have the different work function.[2]

In order to fabricate the inverter devices, grown ZnO NWs were dispersed to the SiO_2/Si substrate by using a drop-and-dry method. The Ni/Ti source and drain electrodes were deposited by e-beam evaporator with a combination of photo-lithography and lift-off process. To make 30nm-thick Al_2O_3 gate insulator layer, we used Atomic Layer Deposition (ALD) system. And then, Pd and Ni/Ti top gate electrodes were deposited and these two devices were connected by wire bonding technique.

The threshold voltage of the Pd top gate ZnO NWs FET shows more positive value (~ 0 V) than that of the other FET (~ -1 V) with Ni/Ti top gate, and these transistors are able to be used as a driver and a load, respectively. The linear mobility of the driver shows about 119 cm^2/Vs at V_D = 0.6 V and the inverter device has high gain value of ~15 at V_{DD} = 5 V. Furthermore, the dynamic property of the logic inverter was measured under the 5 V square input voltages.

More details will be discussed in the meeting.

References

1. G.J, W. K. Hong, J.S. Maeng, M.H. Choe, W.J. Park, and T. K. Lee, *Appl. Phys. Lett*. **94** 173118 (2009)

2. K.M. Lee, J.H. Kim and S.I. Im, *Appl. Phys. Lett*. **88**, 023504 (2006)

8:40am **NS+EM-MoM2 Control of Growth Kinetics for Three-Dimensional III-nitride Nano-Heterostructures Towards Nanowire Devices**, ***S.D. Carnevale***, *P.J. Phillips, T.F. Kent, J. Yang, M.J. Mills, R.C. Myers*, Ohio State University

The geometry of semiconductor nanowires (NWs) allows for both vertical and coaxial heterostructures, while only vertical heterostructures can be formed using planar structures. This is especially important for III-nitride NWs because crystallographic directions in which heterostructures are formed largely determine the magnitude of internal electric fields due to polarization. Here we describe a method to control the relative vertical and coaxial growth rates in catalyst-free GaN/AlN NW heterostructures grown on Si(111) substrates by plasma-assisted molecular beam epitaxy*.

A growth phase diagram is established relating NW density to substrate temperature and III/V ratio. This diagram reveals a reduction in effective growth rate and an increase in nucleation time caused by GaN decomposition. Using this information, a two-step method is developed to independently control NW density from NW deposition time. To begin we nucleate NWs until a small but appreciable density is reached. If deposition continues under these conditions, density will increase over time until reaching a saturation point. To suppress this increase, substrate temperature is increased upon completion of the initial nucleation time. NWs already nucleated continue to grow, but there is no new nucleation, thus controlling density. Additionally, the change in conditions alters growth kinetics, leading to purely vertical NW growth, which allows for the formation of NWs with arbitrarily large aspect ratios and small diameters (~20 nm). Kinetics that favor coaxial growth are also achieved. A low density, high aspect ratio NW array is prepared using the method described above then material is deposited at a lower substrate temperature. The relative coaxial growth rate increases due to lower Ga ad-atom mobility at the lower substrate temperature. Using this dynamic method, we demonstrate multiple period GaN/AlN (2 nm / 2 nm) superlattices along either the vertical or coaxial NW axis, which exhibit atomically sharp compositional profiles. A coaxial, AlN/GaN resonant tunneling diode structure is presented. Large areas of nanowires are processed for electrical measurements without removing them from the Si(111) substrate. Preliminary electrical measurements are provided for both room temperature and low temperature conditions. This work is supported by the ONR under grant N00014-09-1-1153.

* S.D. Carnevale, J. Yang, P.J. Phillips, M.J. Mills,and R.C. Myers. “Three-Dimensional GaN/AIN Nanowire Heterostructures by Separating Nucleation and Growth Processes”. *Nano Letters* 11, 2, pp. 866-871, Jan. 2011.

9:00am **NS+EM-MoM3 III-V Nanowire MOSFETs**, ***L.-E. Wernersson***, Lund University, Sweden **INVITED**

III-V Nanowire transistors are cosidered possible candidates to extend the transistor scaling roadmap. The improved electrostatic control in the cylindrical geometry provides benefits for scaling and the advantageous transport properties of the III-V materials may be used to increase the drive current. Besides heterostructure design may be used to tailor the properties in the transistor channel.

In this talk, we will review some of the efforts made in Lund to realize high-perfromance III-V nanowire transistors using vertical nanowires grown by MOVPE. We will show how bottom-up technologies can be combined with top-down processing to realize nanowire-based RF-devices on Si 2" wafers. We use CV techniques to characterize the properties of the high-k material in vertical nanowire capacitors and compare the data to the 1/f-noise characteristics of scaled transistors to evaluate the influence of the high-k material on the transistor performance. We also show that the transistor channel may be reduced down to a diameter of 15 nm without degradation of the transport properties. Finally, we explore the use of novel materials in the transistor structures as we developed GaSb/InAs heterostructures with excellent Esaki diode characteristics to be used for TFET implementations.

9:40am **NS+EM-MoM5 Optimizing Quantum Efficiency in Quantum Dot Display**, ***S.J. Lim***, *J. Kwon, Y. Oh*, Seoul National University, Republic of Korea, *B.L. Choi, K. Cho*, Samsung Advanced Institute of Technology, Republic of Korea, *Y. Kuk*, Seoul National University, Republic of Korea

In our previous study, we were able to fabricate full-color, 4-inch display made of colloidal quantum dot (QD). Despite such a demonstration of QD light emitting device which is one of candidates for next-generation display, understanding the interface characteristics between QD layer and electron (or hole) accumulation layer is still lacking and further study for improvement of quantum efficiency is essential. Here, we report on a study of scanning tunneling microscopy (STM), spectroscopy (STS) and cathode luminescence induced by tunneling current, performed on individually manipulated QD. We control the distance between two QDs using STM to reveal the mechanism of interaction between QDs. STS measurement showed shift of energy levels as manipulating the distance between two QDs. This result suggests that there exists the optimal distance between QDs for efficient light emission. Besides by making contacts between separated QDs and organic molecules, we simulated contacts between QD layer and electron (or hole) accumulation layer. From these experiments, we could understand excitonic behavior and carrier hopping from QD to QD or surrounding materials. Our findings thus suggest optimal configuration for QD application in display.

10:00am **NS+EM-MoM6 Polarization Engineered 1-Dimensional Electron Gas**, ***D.N. Nath***, *P.S. Park, M. Esposto*, Ohio State University, *D. Brown, S. Keller, U.K. Mishra*, University of California Santa Barbara, *S. Rajan*, Ohio State University

One-dimensional electron gas (nanowire) based devices are of great interest due to their promise in high-performance electronics and other future device applications. However, synthesis and patterning of arrays of nanowires is a challenge in all material systems since both bottom-up and top-down approaches have their own merits and demerits.

Here we report on the demonstration of pure 1-dimensional arrays of electrons with current density up to 130 mA/mm and carrier confinement greater than 100 meV using lateral polarization engineering in N-polar vicinal AlGaN/GaN heterostructures. The width of the atomic terraces characteristic of vicinal surfaces defines the dimensions of the nanowires which are found to exhibit sharp and clear signatures of 1-dimensionality at room temperature making them promising for novel device applications.

We report on devices fabricated on MOCVD grown N-polar AlGaN/GaN HEMT structures on vicinal sapphire substrate (4^0 miscut towards a-plane) with anisotropy in current and channel pinch-off voltages. Channels parallel to the miscut direction pinched off at higher negative gate biases than those perpendicular to the steps and carried more charge as measured by

direction-dependent C-V profiling. An electrostatic model which predicts a saw-tooth energy band profile in the lateral direction has been proposed to explain the charge anisotropy. Each atomic terrace characteristic of the surface morphology of vicinal GaN with its corresponding saw-tooth energy profile is proposed to exhibit quasi-1D confinement. We will discuss the heterostructure/polarization design of structures demonstrating pure 1-D transport in direction parallel to steps.

Gated structures were fabricated to investigate the physics of the system as the Fermi occupation function is varied by varying gate bias. To confirm that the carriers are indeed 1-dimensional, we used direction-dependent small-signal capacitance voltage measurements to probe the density of state function and hence dimensionality of electrons as a function of gate bias. We developed a 2-band model consisting of one 1-D and one 2-D subband to describe the behavior of these wires at room temperatures. The variation of capacitance as well as charge density for a pure 1-D and a pure 2-D system as a function of applied gate bias as predicted by our 2-band model based on density of states matches very well with the data measured experimentally for 1-D and 2DEG respectively. This confirms that the channels created are indeed 1-dimensional in nature. Since 1-D channels are atomic terrace defined, they are promising for eliminating the disadvantages of both bottom-up and top-down approaches.

10:40am **NS+EM-MoM8 Adding New Capabilities to Silicon CMOS via Deterministic Nanowire Assembly**, ***T.S. Mayer***, *M. Li, T. Morrow, J. Kim, B. Won, K. Sun, X. Zhong, K. Liddell, J.S. Mayer, C.D. Keating*, Penn State University **INVITED**

Integrating functionalized nanowires directly onto Si CMOS chips has the potential to combine highly selective and sensitive chemical and/or biological sensing capabilities with electronic signal processing in a single ultra compact, low power platform. Conventional integrated circuit manufacturing methods place considerable limits on the range of and number of different materials and molecules that can be incorporated onto Si chips, making it difficult to realize this goal. This talk provide an overview a new deterministic assembly approach that uses electric field forces to direct many different types of bioprobe-coated nanowires to specific regions of the chip and to provide accurate registration between each individual nanowire and a specific transistor on the chip. This is achieved by synchronizing sequential injections of nanowires carrying different bioprobe molecules with a programmed spatially-confined electric field profile that directs nanowire assembly. Subsequent back-end lithographic and metal deposition processes are then used to electrically and mechanically connect all of the nanowire devices to the Si chip at the same time. Using this technique, individual nanowire device integration yields exceeding 90% have been demonstrated with a less than 1% mismatch across three populations of DNA-coated nanowires for arrays with densities of 106 cm-2. The nanowire-bound DNA retained its ability to selectively bind complementary target strands following assembly and device fabrication showing that this process is compatible with these back-end manufacturing steps. The uniformity in the electrical properties of nanowire device arrays that were fabricated using this hybrid integration strategy will also be discussed.

11:20am **NS+EM-MoM10 Solid-State Dewetting of Direct Nanoimprinted Metallic Thin Films**, ***R. Clearfield***, North Carolina State University, *J.D. Fowlkes*, Oak Ridge National Laboratory, *P.D. Rack*, University of Tennessee Knoxville, *N. Samatova*, Oak Ridge National Laboratory, *A.V. Melechko*, North Carolina State University

Heat applied to thin films below a critical thickness will generally cause transformation of the film into isolated particles. This process is known as dewetting. Solid state dewetting occurs below the melting temperature of the film and is governed by diffusive mass transport. Currently two mechanisms of dewetting are distinguished: hole nucleation and growth, and spinodal dewetting. Spinodal dewetting proceeds via film surface undulations that have characteristic wavelengths related to the thickness of the film. Lithographic patterning of thin films has been utilized to direct the dewetting instability development toward designed nanostructured geometry of nanoparticle arrays. Tailoring the geometry of thin film edge have been shown to affect both heterogeneous nucleation and spinodal dewetting regimes. Nanoimprint lithography, conventionally used for definition of the edges of thin films, is a fabrication method where a stamp is pressed into a thin normally monomer or polymer film at elevated temperatures. Nanoimprinting can also be conducted in direct mode where the stamp is pressed into a metallic film. Surface undulations characteristic for spinodal dewetting will be used to direct the stamp design. Such imprinting allows setting initial conditions, programming instability, in the thin metallic film that is linked to the spinodal surface instability. In this work we are presenting the results of the investigation into behavior of thin films in which a 3D structure has been imprinted. We present observations on the effect of direct nanoimprint lithography on nanoscale Au and Ni films using periodic arrays of cylinders. Our focus is on the spatial distribution of the particles produced from dewetting of the nanoimprinted films. Particles in patterned regions are characterized in terms of their spacing, periodicity and size, and shape. The geometry of the dewetted patterns is compared to that of the 3D features created after direct nanoimprinting of the films. Analysis of spatial correlation of the final dewetted patterns to stamp patterns is presented.

Authors Index

Bold page numbers indicate the presenter