Tuesday Afternoon, November 1, 2011

Nanomanufacturing Science and Technology Focus Topic
Room: 207 - Session NM+NS+MS-TuA

Manufacturable Nanoscale Devices and Processes
Moderator: R. Maboudian, University of California at Berkeley, R. Mu, Fisk University

2:00pm **NM+NS+MS-TuA1 Assessing Nanotechnologies for Volume Manufacturing**, ***B.E. Goodlin***, *S. Butler, L. Colombo, R. Doering*, Texas Instruments Incorporated **INVITED**

Over the past several years, we have seen significant advances in nanotechnology. Much of the underlying purpose of "nanotechnology" research and development, at least as it applies to the electronics industry, is to revolutionize mainstream technology through the use of unique properties and capabilities of nanomaterials, like Si nanowires, graphene, CNTs, in an effort to provide advantages that could not be otherwise obtained thru evolutionary technology scaling. However, the ultimate goal of adopting such technologies into volume manufacturing will most certainly rely on the same tried and tested principles that govern adoption for mainstream manufacturing. Such principles include: performance (does the process hit the desired target?), cost (is it more/less costly as compared to alternatives?), capability (how reproducible is the process?), throughput (how many product can be produced and at what rate?), yield/defectivity, reliability, controllability/metrology (can the process be controlled and what measurements are needed?), maintainability (is equipment/process required easy to maintain?). Do these same governing manufacturing principles truly apply for nanotechnologies? If so, how do some of the current nanotechnologies fare? What gaps exist? Is sufficient focus being applied to address these gaps? Can we even provide adequate answers to these questions yet? Prior to addressing these questions, one must first step back and clearly identify the important, unique requirements (process, materials, equipment) that exist for a given nanotechnology to enable delivery of the desired performance. Also, one must consider interactions and compatibility of the processes with upstream and downstream processes that are necessary for the final product. Have such requirements and interactions been thought out clearly for various nanotechnologies? If so what are the requirements? What are the interactions? This talk will seek to investigate answers to these questions in an effort to assess various emerging nanotechnologies and their capabilities for eventual adoption into volume manufacturing.

2:40pm **NM+NS+MS-TuA3 Material and Tool Design Challenges for Taking ALD to High-volume Production Beyond 30nm Node**, ***B. Lu***, *Z. Karim, S. Ramananthan*, AIXTRON Inc. **INVITED**

Atomic Layer Deposition enables conformal coating of high-quality thin film on complex nano-scale structures. It has been the preferred choice of deposition technology for high-k and metal films in high-aspect ratio capacitor structure for memory applications. Maintaining 25 fF/cell in sub 30nm DRAM devices poses multiple challenges: (a) structural - very high aspect ratio (~100:1) capacitor cell structures and (b) material - the need for advanced Hi-k oxides beyond ZrO2, which are typically multi-component oxides. Chemical precursors for a majority of the promising new high-k materials are typically low vapor-pressure liquids or even solids. Achieving excellent composition control inside these high aspect ratio structures using low vapour pressure precursors is a significant challenge. These challenges are pushing ALD technology to its limit and are testing its production-worthiness for high volume manufacturing of sub 30nm devices. Innovative technology in precursor delivery, reactor design, and platform architecture are required to overcome these challenges. This presentation will discuss the new developments in equipment design to meet the technology needs as well as practical manufacturing targets (such as throughput and cost of ownership) in order to provide a production-worthy ALD solution. Applications in new high-k oxide (La/Sr/Ba oxides), metals, and PCRAM materials (such as GST) will be discussed.

4:00pm **NM+NS+MS-TuA7 The Metal-Oxide-Metal Vacancy Drift Memristor - A CMOS Compatible, High Speed, Non-Volatile Switch for Universal Memory and Storage**, *R.S. Williams*, ***J.P. Strachan***, Hewlett-Packard Labs **INVITED**

The existence of the fourth passive circuit element was proposed by Prof. Leon Chua of UC Berkeley in 1971 from fundamental symmetry arguments to augment the familiar resistance, inductance and capacitance equations. Although he showed that such a 'memristor' had many interesting and useful circuit properties, until 2008 no one knew if such a circuit element existed or not. In fact, researchers had been making and studying memristors for decades without knowing it - examples are resistive RAM devices, STTRAM devices and phase change memory devices. At HP, we have focused primarily on metal-oxide-metal bipolar resistive switches. Memristance arises naturally in these systems via coupling of electronic and ionic transport in thin semiconducting metal-oxide films under an external bias voltage. Simple analytical models show that memristance becomes much more important as the thickness of the active device region decreases, and thus memristors are mainly nanoscale structures. Memristor theory serves as the foundation for understanding a wide range of hysteretic current-voltage behavior, including both unipolar and bipolar switching, observed over the past 50 years. We have built nanoscale titanium dioxide and tantalum pentoxide memristors in our laboratory and have demonstrated both their fundamental electrical properties and several potential uses. They can be integrated into electronic circuits using conventional fabrication techniques and materials available in standard CMOS fabrication facilities. I will discuss recent results on such topics as device switching speed, endurance, measurements required to parameterize a physics-based SPICE model, and 3D stacking of memristive crossbars.

4:40pm **NM+NS+MS-TuA9 Large Scale Graphene: Progress and Challenges**, ***R.S. Ruoff***, The University of Texas at Austin **INVITED**

Graphene-based materials hold promise due to their electronic and thermal transport properties,mechanical properties, high specific surface area, and that they can act as an atom thick layer, barrier, or membrane. Here, I focus on growth of large area graphene on metal substrates and the structure and thermal and mechanical properties of such graphene. A history of experimental work on graphene (from its discovery in 1969 until 2010) is provided at:

http://bucky-central.me.utexas.edu/ .

Support of our work by The WM Keck Foundation, DARPA, ONR, SWAN NRI, NSF, ARO, AEC, and Graphene Energy, Inc., is appreciated.

5:20pm **NM+NS+MS-TuA11 Laser-Assisted Electron-Beam Induced Deposition and Etching**, ***N.A. Roberts***, University of Tennessee and Omniprobe, Inc., *J.D. Fowlkes,* Oak Ridge National Laboratory, *P.D. Rack,* University of Tennessee and Oak Ridge National Laboratory, *G.A. Magel, H.M. Marchman, C.D. Hartfield, T.M. Moore*, Omniprobe, Inc.

Focused electron-beam induced deposition (EBID) and etching (EBIE) are direct-write nanofabrication techniques that allow localized deposition or etching of materials without the need for resists. These deposition and etching processes are controlled by electron-beam dissociation of a precursor gas. In both cases, by-product species are created, and if the unwanted byproduct is not desorbed from the surface it will be incorporated into the deposit or reduce the etch rate for deposition and etching, respectively. Substrate heating has been used in experiments to enhance desorption by reducing the residence time of the by-product. The substrate heating has the same impact on the residence time of the precursor gas and therefore reduces the growth or etch rate of the process. *Ex situ* treatments of deposits have also been investigated to remove impurities with some success, but these treatments results in void formation and shape changes. *In situ* laser processing at short pulse widths is ideal for electron-beam induced processing because desorption of the by-products can be achieved by local heating of the sample, but the narrow pulse width results in a short heating time and cooling time. Thus the by-products can be effectively desorbed and adequate recovery time for fresh reactant to re-adsorb.

Laser-assisted EBID and EBIE processes are made possible through the use of the OptoProbe™, which is an optical imaging and processing system that can be attached to an SEM and used in conjunction with an appropriate gas injection system. The design of this port-mounted optical accessory enables simultaneous optical imaging and delivery of laser irradiation to a sample within the SEM, without interfering with normal SEM/FIB imaging and processing modes. The optical system is mounted on a 3-dimensional nanomanipulator so that precision alignment and focusing is easily achieved. For this work, the OptoProbe™ has been optimized to deliver a high-irradiance near-infrared laser spot to provide localized time-dependent sample heating for enhancing focused electron-beam induced deposition and etching. In this presentation, we will discuss recent experimental results as well as modeling of laser-assisted EBID of Au and EBIE of SiO_x using XeF_2.

5:40pm **NM+NS+MS-TuA12 Channel SiGe Selective Epitaxy Process for DRAM High K Peripheral Transistors***, **J. Yeo**, H. Hwang, S. Lee, W. Yoo, S. Ahn, I. Jeon, B. Kim, S. Nam, S. Kim, K. Jung, J. Lee, S. Jang, T. Lee, K. Huh, S. Yamada*, Samsung Electronics Co., Ltd, Republic of Korea

As the DRAM technology evolved towards the sub 2x era, the need for high performance transistor grows higher for the DRAM peripheral transistors. The novel technologies such as embedded SiGe, high K gate oxide, or 3-dimensional transistor technologies are indispensible in a near future. Especially, to scale the gate oxide further and to meet the gate oxide leakage constraint at the same time, high K gate dielectrics should be adapted. For a successful application of high K dielectrics to DRAMs, it is essential to realize the effective work-function (EWF) for both n, pMOSFETs, where this EWF should be maintained even after huge back-end thermal budget of DRAM process. Therefore, so called 'gate-first approach' has been examined, i.e. LaO, or MgO capping layers for NMOS [1,2], and AlO capping layer, F implantation, and ion implantation on metal for PMOS [2,3], respectively. A SiGe channel has been also examined by many research groups [4-7]. When SiGe epitaxial layer is introduced to the PMOS channel, interface trap density (Dit) has been increased by order of magnitudes, which consequently results in the degradation of transistor performance and reliability [4]. To control this interface degradation, Si capping layers often deposited on the SiGe channels, which reduces the Vt gain that can be gained by SiGe only. In this research, SiGe selective epitaxial growth (SEG) condition has been set-up first, Si capping condition has been optimized by tuning growth temperature, process pressure, and Cl/Si ratio in a LPCVD chamber. The process pressure was precisely controlled to grow Si capping layer 'selectively' as well as to avoid SiGe migration. When we increased the process pressure, surface atomic mobility can be decreased, which effectively reduced SiGe migration. However, when the pressure is increased too high, resulting in growth rate too high, selective growth condition fails. HCl/SiH4 flow rates were also tuned to get a margin for selective growth condition. When introduced to DRAM peripheral transistors, a SiGe channel reduces PMOS Vth by 290 mV, and Si capped SiGe channel by 170 mV, respectively, which has good agreement with the expected value by Energy Band Simulation. This reduced Vt controllability could be recovered by increasing Ge content of SiGe channel. To conclude, the channel SiGe channel SEG process has been successfully applied for DRAM integration, and robust pMOSFET Vt tuner method was realized.

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