

Tuesday Afternoon, November 1, 2011

Graphene and Related Materials Focus Topic

Room: 209 - Session GR-TuA

Graphene on Dielectrics, Graphene Transfer to Novel Substrates

Moderator: A. Turchanin, University of Bielefeld, Germany

2:20pm **GR-TuA2 A Scanning Tunneling Microscopy and Spectroscopy Study of Artificially Modified Bilayer Graphene.** *H. Baek, J. Ha, B. Hwang, J. Kwon*, Seoul National University, Republic of Korea, *J.A. Strosio*, National Institute of Standards and Technology, *Y. Kuk*, Seoul National University, Republic of Korea

Bilayer graphene has drawn considerable attention due to deviation from Dirac Fermion picture such as anomalous quantum hall effect and a tunable band gap in their spectrum. While a pristine Bernal (AB) stacked bilayer graphene can be synthesized by mechanical exfoliation, growth on a SiC single crystal and epitaxial growth on metal substrates, separate control of the top and the bottom layers has seldom been performed. In this study, artificially modified 2D layers were demonstrated with individually stacked bilayer graphene. Large-area graphene was grown on a Cu foil by chemical vapor deposition (CVD). CVD-grown graphene layers were transferred successively onto insulating substrates with minimum chemical process for realizing bilayer graphene. In this method the mosaic spread between the top and the bottom graphene layers could be varied and an additional thin layer structure could be inserted between the two layers. Artificial bilayer graphene was investigated using scanning tunneling microscopy and spectroscopy. In topographic images and spatially resolved spectrums of local density of states, defect scattering and the misorientation between two graphene layers suggesting weak interaction compared to the AB stacking were found.

3:00pm **GR-TuA4 Dry Transfer of Single Layer Graphene to Polymers.** *E.H. Lock, S.G. Walton, M. Baraket, M. Laskoski, S. Mulvaney, W.K. Lee, P.E. Sheehan*, Naval Research Laboratory (NRL), *D. Hines*, Laboratory for Physical Sciences (LPS), *J.T. Robinson*, Naval Research Laboratory (NRL), *J. Tosado, M. Fuhrer*, University of Maryland, College Park

The ability to grow and transfer large area single-layer graphene is critical from both fundamental and applied points of view. The transfer of large area samples will facilitate fundamental studies of graphene's unique properties. It can also allow for the fabrication of three-dimensional structures, electrically insulated graphene bilayers, graphene on previously unexplored substrates and "curved" graphene with non-trivial geometry. Currently, single layer graphene grown via CVD on metal foils is transferred to other substrates via chemical etching of the foil. The transfer process is time consuming, generates chemical waste, and destroys the foils.

We have developed method for direct dry transfer of graphene grown on Cu foils to polymers. The method relies on the differential adhesion between graphene, the metal foil, and the receiving polymer. A successful print results when the adhesion of graphene to the polymer surface is stronger than its adhesion to the metal foil. Plasma treatment of polymers allowed for the attachment of perfluorophenylazide (PFPA) linker molecule. The transfer printing was performed by placing the PFPA treated polymer surface in contact with graphene covered Cu foil and applying heat and pressure. Then, the polymer substrate with transferred graphene was separated from the Cu foil. In this talk, details of the printing process along with graphene film characterization will be discussed.

This work was supported by the Office of Naval Research. M. Baraket appreciates the NRL/NRC postdoctoral research fellowship.

4:00pm **GR-TuA7 Studies on Ozone Based Atomic Layer Deposition of High-k Dielectrics on Graphene.** *S. Jandhyala, G. Mordi, B. Lee, J. Kim*, University of Texas at Dallas, *P.-R. Cha*, Kookmin University, Korea

Graphene, being a two dimensional material, is one of the most promising alternative channel materials for post-Si generation [1-3]. However, being just one atom thick and having an inert surface, it poses a huge challenge to develop a top-gate dielectric process for graphene-based devices. Several techniques are currently being explored for depositing dielectrics including physical-vapor deposition (PVD), chemical-vapor deposition (CVD) and atomic layer deposition (ALD) after chemical 'functionalization' of graphene (using NO₂ or O₃) or after depositing nucleation layers (such as Al, PTCA, PVA) on graphene [3].

Here, we will present a novel technique developed by our group for depositing ALD high-k dielectrics such as Al₂O₃ on graphene through ozone functionalization [4]. Physisorption of ozone has been claimed to be the plausible mechanism for functionalizing the graphene surface [5]. Based on Langmuir adsorption equation, the amount of ozone adsorbed on graphene can be increased by increasing the partial pressure of ozone. By utilizing this, we have been able to precisely control the dielectric thicknesses and successfully scale dielectrics on graphene down to a thickness of ~3 nm. We employed both AFM on HOPG/graphene and in-situ electrical characterization of graphene-FETs in order to understand the adhesion mechanisms of ozone with graphene, enabling the deposition of ALD dielectrics. For in-situ electrical characterization, we used package-level devices with back-gated graphene devices to detect molecules adsorbed on graphene surface. The observed charge scattering mechanisms and effect on mobility due to the interaction of ozone with graphene as a function of temperature and amount of ozone will be presented. In-situ studies regarding the role of TMA (Tri-methyl Aluminum) will also be discussed based on experiments in actual ALD chambers.

Acknowledgement

NRI-SWAN (Theme # 1464.012) and Korea-US International R/D program by MKE

References

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- [4] B. Lee, et al., *Appl. Phys. Lett.*, 97 (4), 043107 (2010)
- [5] G. Lee, et al., *Jour. Phys. Chem. C*, 113 (32), pp. 14225-14229 (2009)

4:20pm **GR-TuA8 Fluorine Functionalization of Epitaxial Graphene for Uniform Deposition of Ultrathin High-κ Dielectrics.** *V.D. Wheeler, N.Y. Garces, L.O. Nyakiti, R.L. Myers-Ward, J. Culbertson, C.R. Eddy Jr., D.K. Gaskill*, U.S. Naval Research Laboratory

Thermal atomic layer deposition (ALD) is a viable approach to attain high-quality ultrathin dielectric films needed for graphene devices, but the hydrophobic nature of the graphene surface inhibits direct application of thermal ALD oxides. Several methods have been explored to render the surface more susceptible to ALD[1-3], but these techniques often result in graphene mobility degradation and/or shifts in the Dirac voltage due to charge in the gate stack. In this work, we investigated a simple dry chemical approach using XeF₂ to functionalize the graphene surface prior to ALD which results in conformal ultrathin high-κ oxides without degradation of the underlying graphene electrical properties. Epitaxial graphene samples were grown on semi-insulating, on-axis (0001) 6H-SiC substrates using an Aixtron VP508 SiC reactor at 1650°C for 120 min. Fluorination of the graphene was performed in a Xactix X₃ etcher operating in pulse mode. Optimum fluorine exposure conditions consisted of six, 20s pulses with constant XeF₂ and N₂ carrier gas partial pressures of 1 and 35 torr, respectively. X-ray photoelectron spectroscopy (XPS) was used to chemically analyze the functionalized surface prior to oxide deposition. ALD Al₂O₃ and HfO₂ films (≤ 15 nm) were deposited at temperatures between 150 - 225 °C using TMA or TEMAHF and deionized (DI) water precursors. Growth was initiated with 20 DI water pulses. Oxide coverage was characterized with atomic force microscopy and scanning electron microscopy, while graphene mobility changes were observed with van der Pauw Hall measurements. Capacitance-voltage (C-V) measurements were conducted on Ti/Au C-V dots to extract the dielectric constant and electrical quality of the oxide. Initial results show that 15 nm conformal, uniform Al₂O₃ and HfO₂ films are obtained with an optimized XeF₂ surface treatment prior to ALD. XPS showed that the optimum XeF₂ treatment resulted in ~6% fluorine on the surface and the presence of only C-F bonds which provide ALD reaction sites needed for uniform oxide deposition. Graphene mobilities were maintained, and occasionally increased, implying little impact of the XeF₂ treatment or ALD oxide on the underlying graphene properties. Raman spectroscopy reveals no change in the D/G ratio after XeF₂ and oxide deposition, verifying that the graphene lattice quality is maintained. The viability of the fluorination method for achieving ultrathin films (<10 nm) will be presented along with electrical C-V data to show the electronic quality of the ALD oxides.

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2. Farmer, et al. *Nano Letters* **9(12)** 4474 (2009)
3. Lee, et al. *ECS Transactions* **19(5)** 225 (2009)

4:40pm **GR-TuA9 Improving Performance of CVD Graphene Field Effect Transistors by Reducing Water Trapped at the Graphene/Substrate Interface.** *J. Chan, A. Venugopal, A. Pirkle, S. McDonnell, D. Hinojos*, The Univ. of Texas at Dallas, *C. Magnuson, R.S. Ruoff*, The Univ. of Texas at Austin, *L. Colombo*, Texas Instruments Inc., *R.M. Wallace, E.M. Vogel*, The Univ. of Texas at Dallas

Graphene grown by chemical vapor deposition (CVD) provides a promising pathway for large area fabrication of graphene field effect transistor (FET). However, the performance of CVD graphene FETs reported to date is poorer than FETs fabricated using exfoliated graphene. CVD graphene FETs often exhibit strong hysteresis accompanied with low mobility, large positive Dirac point (V_{Dirac}) and large intrinsic carrier concentration. CVD graphene is exposed to a number of aqueous solutions and deionized water when it is transferred to a device substrate. We find that the large V_{Dirac} shift and strong hysteresis observed in CVD graphene FET are largely due to water trapped in the graphene/substrate interface during the transfer process.

In this study, CVD graphene grown on copper is transferred to SiO_2 substrates with the following three interfacial conditions: i) normal hydrophilic SiO_2 , ii) SiO_2 with 20nm of Al_2O_3 , and iii) a hydrophobic surface prepared by coating hexamethyldisilazane (HMDS). Device performance, including mobility, V_{Dirac} and intrinsic carrier concentration are compared in ambient as well as in vacuum. Gate hysteresis is analyzed by measurement of time-resolved channel resistance at various back-gate bias voltages. We find that the gate hysteresis is partially reduced by transferring the graphene onto a substrate coated with HMDS. Vacuum pump down and low temperature (80 °C) annealing can remove the remaining gate hysteresis and V_{Dirac} shift. The resulting hole mobility is $5.42\text{cm}^2/\text{Vs}$, which is high compared to most of the CVD graphene mobility values reported in the literature.

As a control experiment, the CVD graphene FET fabricated on untreated SiO_2 shows a smaller mobility, a larger V_{Dirac} and a stronger hysteresis compared to the HMDS coated sample. Under vacuum the hysteresis is reduced but remains significant. We believe the remaining hysteresis is due to adsorbates trapped at the substrate/graphene interface. A graphene FET prepared on a substrate with an Al_2O_3 interface shows less hysteresis than the sample fabricated on an untreated SiO_2 surface but more than that of the HMDS coated surface. In order to study the influence of water trapped between the graphene and the substrate, water is intentionally replaced by isopropanol at the end of the transfer process before drying. In samples prepared using this method, hysteresis and V_{Dirac} point shift are both reduced. These results indicate that efforts to prevent trapping of water molecules at the graphene/substrate interface during the transfer process will improve the performance of CVD graphene FETs.

This work was supported by the NRI SWAN center, ONR, NSF and Sandia's LDRD program.

5:00pm **GR-TuA10 Improved Performance of Top-Gated Graphene-on-Diamond Devices.** *A.V. Sumant*, Argonne National Laboratory, *J. Yu, G. Liu, A. Balandin*, University of California, Riverside

Since the discovery of graphene and realization of its exceptional electronic properties in suspended form, there have been many efforts in fabricating FET-type devices based on single and bilayer graphene on SiO_2 substrate. However, performance of these devices is found to be inferior to the expected intrinsic properties of graphene. It has been observed that apart from carrier mobility in graphene, which is sensitive to trapped charges, and surface impurities at the graphene-oxide interface, breakdown current density in graphene depends sensitively on the heat dissipation property of the underlying supporting substrate. Although graphene has extremely high intrinsic thermal conductivity, it is reported that in graphene devices, more than 70% of the heat dissipates through the 300 nm SiO_2 on silicon directly below the active graphene channel while the remainder is carried to the graphene that extends beyond the device and metallic contacts. Such a distribution of heat in to the substrate cause undesirable effects on the overall performance of the device. We show for the first time that by the use of thin CVD-grown ultrananocrystalline diamond thin films on silicon in graphene-on-diamond configuration, the heat dissipation can be improved substantially leading to the higher breakdown current density of more than 50% as compared to conventional graphene-on-oxide substrates. We also describe the fabrication of the top-gate graphene-on- diamond devices and discuss their performance. The obtained devices had the carrier mobility $\sim 2354\text{ cm}^2\text{V}^{-1}\text{S}^{-1}$ for holes and $\sim 1293\text{ cm}^2\text{V}^{-1}\text{S}^{-1}$ for electrons. The obtained results are promising for developing high-performance graphene-on-diamond devices and interconnects for future electronics.

Use of the Center for Nanoscale Materials was supported by the U. S. Department of Energy, Office of Science, Office of Basic Energy Sciences, under Contract No. DE-AC02-06CH11357. The work in Balandin group at UCR was supported, in part, by DARPA – SRC Center on Functional Engineered Nano Architectonics (FENA).

5:20pm **GR-TuA11 Growth of Turbostratic Graphene on Sapphire.** *S. Rothwell, P.I. Cohen*, University of Minnesota, *M. Kumar*, National Physical Laboratory, India

Large area turbostratic graphene was grown on the (0001) plane of sapphire by thermal decomposition of acetylene. Sapphire is an attractive substrate since it has a symmetry match and close coincidence lattice match to graphene. It is a good insulator, appropriate for electronics applications, and large single crystal wafers are readily available. We have found that only after overcoming nucleation barriers, high quality graphene can be grown directly on sapphire without transfer. The sapphire was first heated to about 1400 C to obtain a reconstructed $\sqrt{31}\times\sqrt{31}$ R9 surface structure. The reconstruction was monitored in real time via reflection high energy electron diffraction, which was possible due to the low Debye-Waller factor. After obtaining a clean reconstructed surface, the sample was cooled to near room temperature and exposed to 10 Torr of acetylene. The sample was then heated to 1400 C in the presence of acetylene, in order to nucleate growth. At these pressures, sufficient acetylene coverage for growth was maintained during the ramp to high temperatures. Continued exposure to acetylene at 1400 C did not result in further growth. We speculate that at high temperature there is not sufficient residence time for incorporation, thus lower temperature is needed for further growth. Controlling pressure and temperature during a cool down phase becomes the fine control for film thickness. For example, 10 nm thick graphene samples were obtained by cooling in $1 - 7\text{ E-7}$ Torr of acetylene. Transmission electron diffraction showed very sharp, nearly continuous rings, indicating large domains and no preferential azimuthal rotation between planes. X-ray diffraction showed an increased layer separation of 0.345 nm compared to graphite. Electron energy loss spectroscopy showed bulk-like plasmons or interband transitions, indicative of multilayer graphene. Raman spectra showed 2D/G peak intensity ratios of 0.5 to 1, comparable to literature values for turbostratic graphene. The spectra also exhibit the expected broader highly symmetric 2D peak. Thicker films could be easily lifted from the substrate. Films greater than 100 nm thick exhibited macroscopic ripples while 10 nm thick films were flat. Hydrogen was explored as a means to control growth but was found to rapidly etch graphene and to passivate the room temperature reconstructed sapphire surface. The growth was modeled with a simple rate equation analysis. These results offer a route to large area graphene grown directly on single crystal sapphire wafers.

Partially supported by the University of Minnesota IREE and by the National Physical Laboratory, India

5:40pm **GR-TuA12 Scanning Tunneling Microscopy and Nanomanipulation of Graphene-Coated Water on Mica.** *J.D. Wood, K.T. He, E. Pop, J.W. Lyding*, University of Illinois at Urbana Champaign

Graphene on ultraflat substrates such as hexagonal boron nitride has shown to suppress charge puddle formation and give high carrier mobility [1,2]. Transfer of graphene to other ultraflat substrates such as muscovite mica might bring about similar transport characteristics. To that end, we place graphene on mica for scanning tunneling microscopy (STM) studies. We grow monolayer graphene on Cu by chemical vapor deposition and support it with polymethyl methacrylate (PMMA). We clean the film with water baths and transfer it to mica. In contrast to previous atomic force microscopy (AFM) experiments of dry-transferred exfoliated graphene on mica [3,4], our graphene films trap multiple water layers. After a 700 °C *in situ* degas, we achieve atomic resolution of graphene on water on mica, and we notice that there are at least 3 layers of ordered, bound water on mica [5], due to the wet transfer and the highly hydrophilic mica. We can atomically image graphene monolayers, bilayers, and grain boundaries regardless of the underlying water structure. Additional water layers on top of the bound water are rough, weakly bound, and amorphous. We notice up to 5 layers of graphene-encapsulated water on mica. Using the STM tip, we can nanomanipulate these amorphous layers at high tunneling conditions ($>6\text{ V}$, 1 nA). These water patterns are highly stable, invariant after several days of scanning. Water nanomanipulation under graphene could help elucidate water's complex bonding structure and charge transfer from graphene to encapsulated species. Further, graphene-coated water can assist in STM-based research of other aqueous-suspended nanostructures.

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