Electronic Materials and Processing Division
Room: 210 - Session EM2-MoA

Dielectrics for Ultra Dense Memory Devices

Moderator: A.C. Kummel, University of California San Diego

2:00pm **EM2-MoA1 Oxides for Spintronics**, ***K.L. Wang***, *P. Khalili, F. Xiu*, University of California Los Angeles **INVITED**

Mainstream CMOS technology in today's electronics continues to scale down in its feature size. However, power dissipation per unit area and variability post two major issues and challenges for the continuing scaling. Spintronics, as an emerging technology that exploits the intrinsic spin of the carriers, could potentially offer power savings, low variability and improved scalability. In the talk, we will address the importance of functional oxides such as MgO in field controlled spin FET devices and magnetic tunnel junctions.

Toward the realization of spin logic devices, electric-field manipulation of ferromagnetism offers a potential for achieving low power dissipation. The control of collection of spins is critical in accomplishing room - temperature s pin field effect transistors for dilute magnetic semiconductors such as MnxGe1-x. We found that by using high-quality MgO as gate oxide, the ferromagnetism of the quantum dots can be modulated up to 300 K, which opens the possibility to build room-temperature spin FETs.In addition, MgO was also shown to be effective for unpinning Schottky barrier height and improving the spin injection. U sing an epitaxially grown Fe/MgO/n-Ge tunnel junction, we have obtained single crystalline and atomically smooth Fe/MgO on Ge. This high quality Fe/MgO/Ge junction not only passivates the Ge surface states to favor electronic transport, but also leads to an enhanced spin injection efficiency due to the symmetry induced spin filtering property of the MgO. By using this junction, we show electrical spin injection to bulk Ge.

We also studied the effect of MgO tunnel barrier thickness on the spin-transfer torque-induced switching of CoFeB-MgO-CoFeB magnetic tunnel junction (MTJ) devices used for nonvolatile memory. We studied the effect of MgO thickness on the resistance-area product (RA) and tunneling magnetoresistance (TMR) of the structures using both film-level current-in-plane tunneling (CIPT) and device-level electrical transport measurements. The TMR showed a large distribution for RA values lower than 4 Ω-μm2 (corresponding to an MgO thickness ~0.85 nm), while it increased to ~150% for larger RA > 6 Ω-μm2. The results allow for optimization of RA and MgO thickness for low write energy and high-density of magnetoresistive random access memory (MRAM) switched by spin-transfer torque (STT). We obtained switching times < 1 ns and write energies < 0.3 pJ for CoFeB-MgO-CoFeB MTJ devices. We also studied the effect of CoFeB free layer composition and thickness on device performance.

2:40pm **EM2-MoA3 Charge Trap Memories and 3D Approaches**, ***G. Molas***, CEA Leti Minatec Campus, France **INVITED**

Charge Trap Memories and 3D Approaches

The standard planar Floating gate Flash memory has been scaled down over 20 years. However, many critical limitations are appearing (charge loss through the top or bottom dielectrics, cell to cell coupling interference, Random Telegraph Noise, reduction of the number of stored electrons, process induced variability…), making difficult further scaling of the memory device.

In this context, charge-trapping memories, based on the TANOS (TaN-Al_2O_3-Si_3N_4-SiO_2-Si) gate stack, are foreseen as the backbone of future NAND technologies, allowing to reach the 20nm era with planar device structures and to overcome the 1X node when coupled to novel 3D vertical memory architectures. Nevertheless, to face this challenging Flash memory evolution, several process innovations are still required, and an in-depth physical understanding of the gate stack material properties, is needed.

This paper discusses the potentialities and limitations of charge trap memories, and proposes some paths of improvements to fulfil the stringent requirements of future memory generations.

First the engineering of the memory gate stack is investigated. In particular, engineered tunnel dielectrics, alternative charge trapping layers and improved control dielectric stacks are proposed, and their impact on the memory performances and reliability is debated. Experimental results are analyzed by means of models and simulations.

Then in a second part, the integration of charge trap memories in 3D architectures is studied. The various approaches investigated in the literatures are reported, and an original method to process stacked 6nm crystalline nanowires with gate all around SONOS configuration is proposed.

3:40pm **EM2-MoA6 A Survey of Cross Point Phase Change Memory Technologies**, ***D. Kau***, Intel Corporation **INVITED**

This survey reviews the current advances in phase change memory and the integrated selector. Based on memory cell configuration in array, there are 3 basic array types, including 2-termanl cross point array [1-6], 3-terminal NOR array [7, 8], NAND string [9]. Among all the configurations, stackable thin-film cross point memory delivers the densest array, therefore the most compact die size. Combining its attributes in cost, performance and reliability, cross point phase change technologies stimulate potential opportunities in computing memory hierarchy.

[1] DerChang Kau *et.al.*, *IEDM Technical Digest*, p617, S27.1 (2009)

[2] Y. Sasago, *et.al.*, *Symposium on VLSI Tech.*, p24, T2B-1 (2009)

[3] K. Gopalakrishnan, *et.al.*, *Symposium on VLSI Tech.*, p205, T19-4 (2010)

[4] Yi-Chou Chen *et.al.*, *IEDM Technical Digest*, S37.4 (2003)

[5] J.H. Oh, *et.al.*, *IEDM Technical Digest*, S2.6 (2006)

[6] Giorgio Servalli, *IEDM Technical Digest*, p113, S5.7 (2009)

[7] Y.N. Hwang, et.al., Symposium on VLSI Circuits, p173 (2003)

[8] Fabio Pellizzer, *et.al.*, *Symposium on VLSI Technology*, p122, (2006)

[9] Y. Sasago, *et.al.*, *Symposium on VLSI Tech.*, T5B-2 (2011)

4:40pm **EM2-MoA9 Resistive Switching in HfO_2 Metal-Insulator-Metal Devices (RRAM)**, ***M. Bonvalot***, Laboratoire des Technologies de la Microélectronique (LTM), France, *C. Mannequin, P. Gonon, C. Vallee*, LTM-CNRS, France, *V. Jousseaume, H. Grampeix*, Minatec, France

HfO_2 is attracting interest as a high-k dielectric for several applications in microelectronics, including transistor and Flash memory gate stacks, as well as Metal-Insulator-Metal (MIM) capacitors for DRAMs and rf circuits. As such, the assessment of HfO_2 reliability is of special importance.

In this work we investigate resistive switching of HfO_2-based devices. The HfO_2 thin films (10 and 20 nm thick) are deposited by the Atomic Layer Deposition (ALD) technique on TiN/Si or Pt/Si wafers (bottom electrode) and top Au electrodes. The MIM devices are subjected to a constant dc voltage stress (CVS) and the current is monitored as a function of time. During these experiments we observe transient leakage currents, followed by a progressive increase of conductivity. Phenomena are related to oxygen vacancy defects. Upon bias application oxygen vacancies drift (space charge limited transient currents) to form conducting filaments (leakage increase) through the HfO_2 thickness. Influence of the electrode is discussed since we found oxygen vacancies in MIM devices to be strongly correlated to the metal oxygen affinity [1]. Identical results have been recently found for TiO_2 RRAM devices [2].

We also proposed to modify the oxygen vacancies and study their effects on the RRAM electrical properties by applying post deposition plasma treatment. Different hydrogen-based (NH_3 and H_2) plasma annealing treatments of the HfO_2 dielectric are carried out in order to study the influence of the oxygen vacancies or defects on the subsequent switching behaviour before the deposition of the top electrode. The RRAM devices are then electrically and physically characterized. I(V) curves are then recorded and switching parameters such the SET voltage are compared for devices with and without plasma treatment. The modifications of switching properties are correlated to chemical analysis results, mainly Angle-resolved X-ray Photoelectron Spectroscopy, Attenuated Total Reflexion (ATR) and Spectroscopic Ellipsometry (SE) up to 8 eV, with special attention devoted to metal/oxide interface investigations.

[1] C. Vallée *et al*, Appl. Phys. Lett. **96** (2010) 233504

[2] J.J. Yang, *et al*, Appl. Phys. A **102** (2011) 785

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