Tuesday Afternoon, November 1, 2011

Electronic Materials and Processing Division
Room: 210 - Session EM-TuA

High-k Dielectrics for MOSFETs Part 2

Moderator: A.C. Kummel, University of California San Diego

2:00pm **EM-TuA1 High Mobility Channel Materials and Novel Devices for Scaling of Nanoelectronics beyond the Si Roadmap**, ***M. Heyns***, IMEC, Belgium **INVITED**

The introduction of high-k dielectrics and metal gates in advanced CMOS has opened the door to Ge and III-V compounds as potential replacements for Si to further increase the device performance. Using MOCVD the selective area growth of low-defect InP and InGaAs layers in submicron trenches on Si was demonstrated. These virtual Ge-III/V substrates can be processed in a standard CMOS line. Short channel Ge pMOS devices with high drive currents were fabricated. Strain engineering using GeSn source/drain areas allows to boost the performance of these devices so that they can outperform their strained Si counterparts. One of the key problems in developing III/V devices is the near midgap Fermi level pinning associated with the high density of defect states present at the high-k/III-V interface. The origin of these states is still under debate but there are clear indications that there exists a strong relationship with native antisite point defects. Various sulfide and other treatments were investigated to passivate the surface. The measured distribution of interface states and border traps on typical III/V MOS structures has some special consequences on the electrostatic operation of different transistor designs. Since inversion mode devices do not seem to be the appropriate choice for III/V based logic applications, other device types have been explored. The Implant-Free Quantum Well (IF-QW) device enables VLSI-compatible processing by self-aligned source/drain definition. Strained Implant Free Quantum Well Ge-based pFETs show excellent short channel control and record drive currents. The concept was also used to demonstrate high mobility n-channel InGaAs devices. For III/V pMOS devices GaSb is at present the material of choice. Very encouraging results have been obtained on direct heteroepitaxy of GaSb epilayers on InP(001) combined with *in-situ* deposition of an Al_2O_3 high-κ gate dielectric. The introduction of these advanced materials also allows the development of new device concepts that can fully exploit the properties of these new materials. Tunnel-FETs, where the III/V material may be either introduced only in the source or in the complete device, can provide superior performance at lower power consumption by virtue of their improved subthreshold behavior, allowing to reduce the supply voltages. Vertical surround gate devices can be produced from III/V nanowires directly grown on silicon, allowing the introduction of a wide range of III/V materials and functionalities on Si. This illustrates some of the possibilities that are created by the combination of new materials and devices to allow scaling of nanoelectronics beyond the Si roadmap.

2:40pm **EM-TuA3 Local Profile of the Dielectric Constant Near the Oxygen Vacancy in the GeO_2 Films**, ***J. Nakamura***, *M. Tamura*, The University of Electro-Communications (UEC-Tokyo), Japan

Ge-based metal-oxide-semiconductor (MOS) devices are focused as complementary-MOS devices for the next-generation in the post-Si technology. However, the dielectric properties of GeO_2 gate ultrathin films have not been clarified yet in detail. Our purpose is to clarify the spatial variation of the local dielectric constant for the GeO_2 thin films using first-principles ground-state calculations in external electric fields [1,2]. In particular, we reveal the local profile of the dielectric constant near the oxygen vacancy in the film, focusing on the crystal phase dependence.

We have adopted quartz (0001) and rutile (001) films with/without oxygen vacancies, in which Ge atoms at the topmost surfaces are terminated with H atoms. We have evaluated the optical and the static dielectric constants that are attributed to the electronic polarization and both the lattice and electronic polarizations, respectively.

From the local profile of the dielectric constants for the ideal films, it has been clarified that the dielectric constants change gradually from the surface and approach constant values at the center of the film. Such features have also been confirmed for the Si and SiO_2 films [1,2]. The dielectric constant for the defective model of the quartz film becomes larger locally "at" the oxygen vacancy site compared with that for the ideal model, but at "adjoining" oxygen sites to the vacancy for the rutile film. Such features stem from the difference in the fashion of the chemical bonding between Ge and O atoms: The dielectric constant for the defective quartz model becomes large at the vacancy site where the covalent Ge-Ge bonding is formed. For the rutile, on the other hand, the Ge-O bondings surrounding the vacancy site are softened because of their less ionic character, which results in the larger displacement in external electric fields, leading to the larger lattice polarization around the vacancy.

[1] J. Nakamura *et al*., J. Appl. Phys. 99, 054309 (2006); Appl. Phys. Lett. **89**, 053118 (2006)

[2] S. Wakui *et al.*, J. Vac. Sci. Technol. B **26**, 1579 (2008); ibid 27, 2020 (2009).

3:00pm **EM-TuA4 Two Step Passivation and ALD Monolayer Nucleation on Ge(100)**, ***T. Kaufman-Osborn***, *J.S. Lee, K. Kiantaj, W. Melitz, A.C. Kummel,* University of California San Diego, *A. Delabie, S. Sioncke, M. Caymax, G. Pourtois*, IMEC, Belgium

Germanium is a promising channel material for next generation MOSFET. The best method to passivate Ge(100) is to form a layer of GeO_2, free of Ge suboxides, using high pressure O_2 or O_3. However, there are three challenges: (1) it is difficult to keep a stoichiometric GeO_2 monolayer (ML) at elevated temperatures, (2) the thermal oxidation process creates a rough interface degrading mobility at high field, and (3) scaling the passivation layer to only 1 ML is a challenge. This study presents a process to form a ½ ML of Ge-H and ½ ML of Ge-OH bonds without disrupting the Ge(100) surface. In-situ scanning tunneling microscopy (STM), in-situ scanning tunneling spectroscopy (STS), and in-situ X-ray photoelectron spectroscopy (XPS) were employed to determine the atomic and electronic structure of the passivation monolayer.

Using a differentially-pumped H_2O dosing system, an ordered, flat monolayer of H_2O chemisorption sites on Ge(100) was formed with a low density of unreacted dangling bonds at 300K. STS data showed that the Ge-H and Ge-OH sites removed the bandgap states from the Ge(100) dangling bonds. Annealing the surface between 20°C and 250°C gradually decreased the coverage of H_2O sites. However, even at 300K, the H_2O surface is highly reactive to trimethyl aluminum (TMA) since it contains a half monolayer of Ge–OH which catalyzes the breaking of Al-CH_3 bonds thereby inducing the formation of Al-O bonds, and the Ge-H sites block ALD ligand chemisorptions. STM experiments showed that the H_2O chemisorbed Ge surface provides a half monolayer of nucleation centers with approximately 0.5 nm spacing for TMA dissociative chemisorption at 300K. High resolution XPS experiments indicated that thermally unstable Ge-OH bonds were converted to thermally stable Al-O bonds. Furthermore, passivating the surface with H_2O prior to TMA dosing doubles the aluminum coverage compared to the TMA only dosed Ge(100) surface. The higher nucleation density from the two step functionalization process, TMA + H_2O, should be favorable for pinhole reduction. DFT calculations are consistent with the data showing TMA reaction with either –Ge-H and –Ge-OH is exothermic, but the reaction of TMA on the –Ge-OH site has both a low activation barrier and higher exothermicity (-41.4 kcal/mol) compared to TMA reaction on the –Ge-H site (-10.8 kcal/mol). The calculation is consistent with the key to full monolayer nucleation, the formation of a full monolayer of Ge-OH chemisorption sites, which is being studied with HOOH dosing.

4:00pm **EM-TuA7 Bilayer High-k Gate Stacks on Ge and InGaAs**, ***P.C. McIntyre***, Stanford University **INVITED**

Research on novel channel materials such as Ge and InGaAs for high performance MOSFETs prompts interest in alternative high permittivity gate dielectrics because the thermal stability requirements that led to the adoption of HfO_2-based high-k dielectrics on silicon are relaxed for such channels. We have focused recently on ALD-grown TiO_2/Al_2O_3 bilayer dielectrics that combine large band gap Al_2O_3 interfacial layers (1-2 nm in thickness) with physically thicker but very high k TiO_2 gate dielectrics as a means of scaling gate capacitance and gate leakage current. This bilayer structure relies on the electrical passivity of the Al_2O_3/channel interface to achieve high performance. This presentation will summarize the scaling potential of these bilayer dielectric structures and methods by which low defect density Al_2O_3/Ge and Al_2O_3/InGaAs interfaces can be prepared.

4:40pm **EM-TuA9 Effect of Post Deposition Anneal on the Characteristics of InP MOS Capacitors with High-k Dielectrics**, ***R.V. Galatage***, *B. Brennan, H. Dong, D.M. Zhernokletov, C.L. Hinkle, R.M. Wallace, E.M. Vogel*, The University of Texas at Dallas

Due to high defect density between III-V semiconductors and high-k dielectrics, buried channel structures with InP barrier layers are being considered for CMOS applications1,2. It has been observed that sulfur passivated InP is thermally stable up to ~460° C3. However, little work has been performed to understand the thermal stability of the high-k/InP interface. In this work, the effect of dielectric post deposition anneal (PDA)

on InP MOS capacitors with high-k dielectrics was studied. Temperatures above 450° C result in an increase of the interface trap density.

MOS capacitors were fabricated on both n-type and p-type InP substrates with HfO2 and Al2O3 dielectrics. Room temperature ammonium sulfide was used for surface passivation prior to ALD. Various temperatures ranging from 400° C to 500° C were used for PDA and a control sample without any PDA was used. The surface Fermi level is severely pinned for the p-InP substrate4 and the device does not go into accumulation. This behavior is not observed for the n-InP substrate. Room temperature C-V characteristics for HfO2/n-InP devices show increased interface trap response for the samples with PDA above 450° C. However, low temperature (77 K) C-V measurements show that the samples with PDA have similar *equivalent oxide thickness (*EOT) and their interface trap response can be compared directly. A semi quasi-static method is used to calculate the Dit distribution across the InP band gap. Details of the technique will be presented. The Dit distribution shows a peak located at mid gap for all of the samples which increases with increasing temperature. A similar trend is observed for Al2O3/InP MOS capacitors. Correlation of these results to X-ray photoelectron spectroscopy (XPS) analysis will be presented.

This work is sponsored by SRC FCRP MARCO Materials Structures and Devices Center and the National Science Foundation.

[1] M. Radosavljevic et al., IEDM Tech. Dig., pp.13.1 (2009).

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[3] A nderson, G. W.; Hanf, M. C.; Norton, P. R.; Lu, Z. H.; Graham, M. J., Appl.Phys. Lett, vol.65, no.2, pp.171-173, Jul 1994

[4] Hyoung-Sub Kim, I. Ok, M. Zhang, F. Zhu, S. Park, J. Yum, H. Zhao, Jack C. Lee, and Prashant Majhi, Appl. Phys. Lett. 93, 102906 (2008)

5:00pm **EM-TuA10 ALD Half Cycle Study of HfO_2 on InP by *In Situ* XPS**, ***H. Dong***, *D.M. Zhernokletov, B. Brennan, J. Kim, R.M. Wallace*, University of Texas at Dallas

InP attracts significant attention as a high mobility channel material for Metal-Oxide-Semiconductor Field Effect Transistors (MOSFETs)-with many excellent electrical measurements reported on InP based devices. It is well known that one of the electrical limitations of surface channel III-V MOSFETs comes from the interface defects generated from surface/interface oxidation between high-k dielectrics and III-V materials, which can cause Fermi level pinning [1]. InP is also considered as a potential buffer layer material for quantum well FETs, which is in direct contact with a gate dielectric [2]. To examine the interfacial chemistry for high-k/InP, we present a half cycle Atomic Layer Deposition (ALD) study on native oxide and wet chemically treated InP (100) samples with Hf (TDMA-Hf precursor) and water by *in-situ* monochromatic X-ray photoelectron spectroscopy (XPS). The "clean up" effect is examined and compared to the results for ALD Al2O3 on InP. The significant reduction of interfacial oxides by pre-ALD wet chemical treatments and the detailed growth rate of HfO2 on various samples are also discussed.

This work is supported by the FCRP MSD Focus Center and NSF (ECCS-0925844).

[1]. W. Wang, C.L. Hinkle, E.M. Vogel, K. Cho, R.M. Wallace, Microelectron. Eng. (2011) doi: 10.1016/j.mee.2011.03.053.

[2]. M. Radosavljevic et al, *IEDM*, Tech. Dig., pp.13.1 (2009).

5:20pm **EM-TuA11 Nonvolatile Memresistive Nano-Crossbar Switches in Pt/Ta2O5/Cu Solid Electrolytes**, ***P.R. Shrestha***, *K.P. Cheung*, National Institute of Standards and Technology (NIST), *H. Baumgart*, Old Dominion University

Metal filament resistive memory is an excellent candidate for a nanoscale crossbar switch, and such two terminal "memresistive" devices are being considered for next-generation non-volatile memory due to the inherent simplicity, scalability and low cost (1). Additionally, these devices show potential to replace static random access memory (SRAM) as high performance switches for reconfigurable devices .

Memresistive devices operate by changing resistance from high (Roff) to low (Ron) values in response to an applied voltage. Despite a tremendous amount of work in the scientific literature, the actual underlying switching mechanism has yet to be fully explained. Few studies, most of which lack measurement details, have reported on the transient current response and high speed switching characteristics of memresistive devices. The papers suggest the presence of the variety of active current and thermal dissolution of the low resistance filament while switching OFF. The switching ON has been attributed to the movement of the metal ions towards the cathode and being neutralized by the electrons to form the metal filament. Transient current measurements for switching ON have not yet been analyzed in detail in the literature. Another crucial problem in measurements of these devices is due to the preferred values of Ron(<1kΩ) and Roff(>1GΩ). Thus the key obstacle preventing fundamental understanding has been the lack of reliable and accurate measurements of the transient response while switching ON (from Roff to Ron). In this work, we developed a new measurement capability that enables reliable and accurate investigation of the transient switching response, monitoring change from low Ron to high Roff.

In order to address the need to reliably and accurately monitor the device I-V transient response extremely fast, we have designed an amplifier with low-gain and high bandwidth (1.7 GHz) to accommodate much faster (and realistic) "program" voltage pulses. For switching purposes, this amplifier allows for fast transient current monitoring during programming with proficiency but not limited to follow 2 nsec of pulse rise time. The high gain bandwidth of the amplifier allows us to monitor change from low current (Roff) to high current (Ron) accurately.

1. R. Waser, R. Dittmann, G. Staikov, K. Szot, Advanced Materials 21, 2632 (2009).

5:40pm **EM-TuA12 Metrology for Interfaces and Mass Transport in C-MOS Related Nanofilms**, *A. Herrera-Gomez,* ***A. Sanchez-Martinez***, *O. Ceballos-Sanchez, M.O. Vazquez-Lepe,* CINVESTAV-Unidad Queretaro, Mexico, *P. Lysaght*, SEMATECH

Interface layers play a fundamental role in determining the electrical properties of CMOS devices because their thicknesses are of a magnitude comparable to that of the dielectric layers currently employed. The main (top) techniques traditionally used for characterizing the chemical depth profile of MOS structures have been XPS-Sputter and Back-Side TOF-SIMS. However, they lack the appropriate resolution to characterize the thickness and composition of nano or sub-nano layers. Due to the lack of appropriate metrology methods, the structure of interface layers is usually assessed indirectly through their effect on the device's capacitance. Another important issue in the processing of MOS devices is the diffusion control of chemical species. To quantify or to simply observe displacements on the order of 2 or 3 nm of low concentration elements with those techniques *is close to impossible*. The semiconductor industry will greatly benefit from a metrology method capable of: (a) characterizing the thickness and composition of the various layers constituting a MOS device, including the interface layers; (b) assessing the effect of process driven diffusion of various critical chemical species present in the film. There is a growing consensus that X-Ray Photoelectron Spectroscopy (XPS), specifically Angle-Resolved XPS (ARXPS), has the appropriate chemical and depth resolution for assessing the depth profile of films between 0 and 8 nm. The precise methodology for applying the technique, however, varies wildly among different groups. In many cases the analysis algorithms of ARXPS data are highly susceptible to noise. Because of this, ARXPS is frequently regarded as qualitative techniques. In this talk we briefly describe a robust ARXPS analysis methodology that *minimizes* the sensitivity to noise. This methodology has been successfully applied to characterize various systems. One example that will be addressed regards the failure mechanism for the degradation of the electrical performance of TiN/HfO2/InGaAs devices during thermal processing. We investigated the change on the structure caused by annealing, such as the possible formation of As, Ga or In oxides, accumulation of these elements in the dielectric, formation of metallic arsenic, and/or any other change on the structure that could be correlated to device degradation. ARXPS experiments were performed on those samples and analyzed using the robust methodology. One important finding was that indium diffuses through the dielectric all the way into the metallic layer upon annealing.

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