Electronic Materials and Processing Division
Room: 210 - Session EM-MoM

Dielectrics for Novel Devices and Process Integration
Moderator: S. King, Intel Corporation

8:20am **EM-MoM1 Surface Cleaning and Monolayer Seeding for ALD of High-k Studied by In Situ STM, STS, and XPS**, ***W. Melitz***, *T. Kent, J. Shen, A.C. Kummel*, University of California San Diego

Air exposed III-V surfaces nearly always defects which prevent full modulation of the Fermi level thereby impeding their use in practical semiconductor devices such as MOSFETs. For a high speed device, the air induced defects need to be removed to reduce trap states while maintaining an atomically flat surface to minimize interface scattering thereby maintaining a high carrier mobility. For silicon, the only commercial atomic layer deposition (ALD) high-k fabrication process is a replacement gate process to avoid processing induced damage. Surface channel III-V MOS devices can be fabricated with ALD high-K gate-first processes; while ALD is known to greatly reduce surface contaminants, contamination removal is not complete and the order of the surface after ALD cleanup is unknown. Using in-situ scanning tunneling microscopy (STM) and scanning tunneling spectroscopy (STS) the surface morphology of a multistep process was explored for gate-last unpinning of air exposed InGaAs and InP surface via cleaning with atomic H and ALD nucleating/passivating with trimethyl aluminum (TMA). STM of atomic H cleaned surfaces shows the dosing temperature and a post deposition anneal are critical to forming surfaces that resemble the decapped InGaAs or a highly ordered InP surfaces. For InGaAs(100), 300K H dosing can produce large multilayer etch features which cannot be annealed out; however by dosing at elevated temperatures these features can be avoided. After H cleaning at 380^{o}C, the surface contains dark features consistent with monolayer etch pits, and these features are reduced by a factor ~50 with a post deposition anneal. The H cleaned and annealed surface can be unpinned by a half cycle dose of TMA followed by annealing because it generates an ordered dimethyl aluminum layer providing monolayer nucleation density, and an atomicly flat surface, critical for aggressive EOT scaling. For InP, a low dose of H at similar temperatures and post deposition anneal generates a mixed surface reconstruction; however, with a higher dosing temperature around 440^{o}C and post deposition anneal around 470^{o}C, a single surface reconstruction is observed. A similar atomic H cleaning and TMA dosing procedure has been demonstrated to produced an ordered passivation layer on air exposed InP(100). It has been shown that for InGaAs and InP an oxide free surface can be achieved with atomic H dosing and annealing, however there is a dependence of surface roughness and defect densities on dosing and annealing conditions. The combination of atomic H cleaning and TMA dosing provides a flat ordered surface ideal as a template for ALD of high-k gate dielectrics.

8:40am **EM-MoM2 Selective Area Regrowth of Self-Aligned, Low-Resistance Ohmic Contacts on InGaAs**, ***J.J.M. Law***, *A.D. Carter, G.B. Burek, B. Thibeault, M.J.W. Rodwell, A.C. Gossard*, University of California, Santa Barbara

As electronic device areas scale with each generation by 1:4, resistances must remain constant, so contact resistivities must scale by 1:4. The high dopant concentrations achievable by molecular beam epitaxy (MBE) provide a method for creating low-resistance ohmic contacts; however, line-of-sight deposition and low desorption of atomic species may hinder the self-alignment of such regrowth. Careful control over growth conditions makes MBE a suitable technique for creating self-aligned, low resistance ohmic contacts to InGaAs.

Samples were grown by solid source MBE lattice matched to semi-insulating InP with layer structure as follows from the substrate: 400 nm InAlAs, 3 nm of Si-doped 2 and 3×10^{19} cm^{-3} InAlAs, and 25 and 15 nm of InGaAs, respectively. 300 nm of SiO_2 and 20 nm of Cr were deposited by PECVD and e-beam evaporation. A combination of electron beam and photolithography followed by ICP dry etching was used to define dummy spacer pillars. Oxidation and oxide removal of exposed InGaAs was done with UV o-zone and a dilute 10 H_2O:1 HCL dip. Samples were heated to 420 °C and treated with thermally cracked hydrogen (≈1×10^{-6} Torr) for 40 minutes prior to regrowth. 70 nm of 5×10^{19} Si-doped InAs was grown on the exposed InGaAs regions with quasi-migration enhance epitaxy (MEE) at 500 °C with V:III beam equivalent pressures of 4.0, 5.6, and 8.0. After regrowth, shorts over the dummy pillar were removed, and samples were metalized with lifted-off e-beam evaporated Ti/Pd/Au and mesa isolated. Contact resistances were extracted by transmission line measurements (TLM).

RHEED images during regrowth showed 4x2 surface reconstructions for regrowths with V:III ratios of 4.0 and 5.6 indicating a group In-rich surface reconstruction. SEM of regrowths at V:III ratios of 4.0 and 5.6 showed no faceting and fill-in to the dummy pillar edge. AFM showed roughened surfaces possibly due to high Si incorporation and lattice mismatch between InGaAs and InAs. Regardless of the V:III ratio during growth, 25 nm thick InGaAs channels showed contact resistances of 190 Ω μm while 15 nm thick InGaAs showed contact resistances of 105 Ω μm. Metal-semiconductor contact resistances were 2.1 Ω μm. Local electrode atom probe shows that the regrowth carries some of the Ga along with it creating a varying InGaAs alloy concentration throughout the regrowth.

9:00am **EM-MoM3 Boron Nitride Development and New Applications for sub-20nm Device Fabrication**, ***M. Balseanu***, *L.Q. Xia, V. Nguyen, M. Naik, D. Cui, K. Zhou, J. Pender, B. Mebarki*, Applied Materials, Inc. **INVITED**

The continuous need for films with lower dielectric constant, higher strength, and greater etch resistance drives the need to explore new materials. In this paper we present a study of boron nitride and other boron-based materials for multiple applications in semiconductor devices discussing the benefits and integration challenges.

As critical dimensions shrink and RC delay increases, the dielectric constant of the interconnect is a continuous area of focus. The current silicon carbo-nitride (SiCN) Cu barrier film has a dielectric constant greater than 5.0 and relatively poor step coverage. Significant advances have been made in recent years to develop a low k, conformal and manufacturable BN thin film for Cu barrier applications. The BN film was shown to have improved leakage, mechanical properties and insensitivity to UV cure relative to SiCN.

Back-end of line patterning has increased in complexity with the introduction of ultra-low k (ULK) dielectric materials. Dual hardmask (HM) patterning scheme eliminates the ULK damage caused by photoresist strip process. The TiN HM has faced challenges in extending below 20nm due to post etch residue and high stress leading to line bending. A boron-based HM material was developed to address those integration challenges. The new material has a low and tunable stress eliminating the line bending concerns. Boron content was optimized for the best selectivity to ULK without impacting the film stress. Significant defectivity and queue time improvement was observed with the boron-based HM due to volatility of the etch byproducts. 9% RC reduction relative to the conventional tri-layer patterning scheme was measured using 45nm 2-metal level electrical test structures.

Double or quadruple patterning technique is required for critical dimensions reduction due to the lack of manufacturable EUV lithography. Spacer-based double patterning (SADP) is one of the most adopted process flows to generate one-dimension regular array structures. Its implementation is impacted by the poor step coverage of the conventional PECVD SiN spacer leading to metal line cuts after final polishing step. A low temperature BN film with superior step coverage, minimum pattern loading, good uniformity and low cost was developed for 20nm node and beyond. Its benefit for SADP was verified using a 20nm half pitch logic structure where a 200mm long serpentine yield was improved by 80%.

Evaluation of the boron-based thin films for Cu barrier and patterning applications has shown their potential to replace the conventional materials used today in the logic and memory process flow and thus enabling scaling below 20nm.

9:40am **EM-MoM5 Novel Organosilicate Polymers for Ultralow-Dielectric Films with High Modulus, Low CTE, and Closed-Pore Morphology**, ***D.Y. Yoon***, *J.H. Sim*, Seoul National University, Korea, *M. Liu*, University of Michigan, *H.W. Ro, C.L. Soles*, National Institute of Standards and Technology, *D.W. Gidley*, University of Michigan **INVITED**

Novel organosilicate polymers are prepared using porogen bridged comonomers for ultralow-dielectric constant insulator applications. We synthesize silsesquioxane based terpolymers with methyltrimethoxysilane, ethylene bridged silane (1,2-bis(triethoxysilyl)ethane) and a porogen bridged silane comonomer via sol-gel reaction. The conventional route to generate nanoporous organosilicate films is to blend in a low molecular mass porogen that phase separates from the organosilicate network into isolated nanoscale domains that template the pores. However, using this approach it is difficult to achieve isolated nanopores with diameters below 2 nm when the total porosity becomes greater than 20 % by volume, which is essential for obtaining ultralow-k (k<2.2) films. Our novel approach here is to covalently tether the both terminal ends of linear organic porogen to

the trialkoxysilane monomers. This helps minimize the phase separation of the porogen during the thermal curing process of organosilicate polymers and keeps the resultant pores both smaller and less interconnected. For comparison we also prepare an analogous grafted version of this terpolymer series where only one end of the linear porogen is tethered to a trialkoxysilane monomer. The pore structures and porosities of this series of bridged and grafted porogen films are fully characterized with positron annihilation lifetime spectroscopy (PALS) and X-ray porosimetry (XRP). The resulting nanoporous films from the porogen bridged organosilicate polymers show much smaller pore sizes (1 nm to 2 nm), reduced interconnectivity of the pore structure, and superior mechanical properties in comparison with their analogs using the porogen grafting approach, especially at the high porosities (ca. 30 %) that are relevant for ultralow-k (2.0 to 2.2) insulators for advanced microprocessor applications.

10:40am **EM-MoM8 Interface Traps and Low Subthreshold Swing in III-V Tunnel FETs**, ***A. Seabaugh***, *S.-D. Chae, P. Fay, W.-S. Hwang, T. Kosel, R. Li, Q. Liu, Y. Lu, T. Vasen, M. Wistey, H. Xing, G. Zhou, Q. Zhang,* University of Notre Dame, *R.M. Wallace*, University of Texas at Dallas **INVITED**

Tunnel field-effect transistor (TFETs) are metal-oxide semiconductor (MOS) devices that use the gate electrode to control the band-overlap of a Zener tunnel junction. In TFETs, the subthreshold swing can be less than the thermal limit of 60 mV/decade in MOSFETs, allowing lower supply voltages for the same on/off current ratio, and lower power dissipation. Traps, however, at the high-k-dielectric/semiconductor interface act to terminate the gate field without contributing charge carriers to the channel and thereby degrade the subthreshold swing. This presentation will examine the relationship between interface traps and subthreshold swing and show, through impedance and transport measurements on InAs/AlGaSb TFETs, our current understanding of the interface, physics, charge control, and channel transport.

11:20am **EM-MoM10 Impact of Vertical Structured Devices for Future Nano LSI**, ***T. Endoh***, Tohoku University, Japan **INVITED**

For the past thirty years, the device downscaling has been the guiding principle in Si-LSI. The planar MOSFET has supported the expansion of the semiconductor industry; however, recently, the limit of planar MOSFETs is becoming apparent. As the feature size of planar MOSFETs approach the nano generation, it is becoming more difficult to improve its performance by SCE etc. Moreover, the process cost becomes expensive. In order to extend the scalability of CMOS technology to the nano generation; a new device structure is necessary. From above viewpoint, many new structured MOSFETs are proposed. The key points of next generation MOSFET are multi-gate structure, floating body structure and 3D structure. Therefore, proposed Vertical MOSFET [1-2] is emerging as one of the candidate to replace the conventional MOSFET.

In this paper, I will show the excellent performance of Vertical MOSFETs in comparison with others structured MOSFETs from viewpoints of high packing density and large driving current and good gate controllability etc. Moreover, I will show the impact of Vertical MOSFET for high density Memory [3].Next, I will discuss that by using both proposed Vertical MOSFETs[4] and Spin device, Silicon ULSI can be evolved even if becoming in nano generation in forces to Logic. Logic demands new scheme technology for realizing lower power operation and managing the total power consumption. On the other hands, Memory, especially non-volatile memory demands new cell technology for shrinking cell size and realizing high speed programming, low voltage operation and good reliability including endurance. From above viewpoint, we will show the excellent performance of both Logic-in-Memory Architecture [5-7] using MTJ, and MTJ based Vertical structured cell, as follows. First, it is shown that by Logic-in-Memory Architecture using MTJ, a compact LSI with a standby-power-free and immediate-power-up capability can be realized. Next, it is shown that by Vertical structured cell using MTJ, ultra high density non-volatile memory can be realized with utilizing both a capability of Vertical structure MOSFET such as large drive current, excellent gate controllability and compact footprint, and a capability of MTJ such as unlimited endurance and manufacturability integrated in backend metal line of Silicon CMOS technology. Finally, we discuss the impact of spintronic devices for future Nano Si-LSI.

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