Monday Afternoon, October 18, 2010

Plasma Science and Technology
Room: Aztec - Session PS1-MoA

Advanced FEOL / Gate Etching I

Moderator: A. Metz, TEL Technology Center America

2:00pm **PS1-MoA1 Reduction of Plasma Induced Silicon-Recess During Gate Over-Etch Using Synchronous Pulsed Plasmas**, ***M. Darnon***, *C. Petit-Etienne, F. Boullard, E. Pargon, L. Vallier, G. Cunge, P. Bodart, M. Haass,* CNRS-LTM, France, *S. Banna, T. Lill*, Applied Materials Inc.

With the downscaling of CMOS devices in semiconductor industry, very thin layers (<1.5nm) are now introduced in transistor gate stacks. Integrating such thin layers presents tremendous challenges, particularly for the etch processes which have to be stopped selectively without inducing damage to the thin materials below. For instance, bulk silicon may be oxidized during the gate over-etch step through the thin gate oxide, which leads to silicon recess during the subsequent wet cleanings. In this contribution, we will precise the mechanisms of silicon oxidation through the thin gate oxide, and we will propose solutions to minimize this phenomenon by pulsing the plasma.

The experiments are performed on a state of the art 300mm AdvantEdge™ etch reactor equipped with the Pulsync™ system which provides full plasma pulsing capabilities at frequencies between 100 Hz and 20 kHz, with duty cycles between 10 and 90 %. In-situ spectroscopic ellipsometry is used to determine etch rates on thick silicon oxide and polysilicon layers, and to investigate plasma induced oxidation through a 2.5nm thin silicon oxide coated on bulk silicon. An angle resolved XPS system connected to the reactor allows quasi in-situ surface characterizations.

We show that an infinite selectivity of polysilicon over SiO_2 is obtained using an HBr/O_2/Ar gate over etch process on thick layers. However, when a thin layer of silicon oxide is exposed to the same process, the thin oxide layer thickness increases with the plasma exposure time. This thickness increase is related to plasma induced oxidation through the thin gate oxide. XPS analysis show that a Si-Br_x interface layer builds up between SiO_2 and Si, and that some bromine is incorporated in the oxide. This suggests that bromine implantation through the SiO_2 layer may generate a path in the oxide layer facilitating the oxygen and water diffusion (from the plasma or from the atmosphere) down to the SiO_2/Si interface

We show that plasma induced oxidation can be minimized by using synchronous pulsed plasmas. This way, we move from a highly dissociated plasma to a highly recombined plasma. As a consequence, radicals are larger and less prone to diffuse, and ions are molecular rather than atomic, which decreases the net energy of their components. Hence, bromine incorporation is highly limited and no Si-Br_x interface layer is created, which minimizes silicon oxidation through the thin gate oxide.

These experiments clarify the mechanisms of plasma induced oxidation through the thin gate oxide, and show the promises of synchronous pulsed plasmas to reduce silicon recess.

2:20pm **PS1-MoA2 Control of Si Damage in Dry Etch Beyond 22nm Technology Node**, ***J. Guha***, *C. Lee, V. Vahedi*, Lam Research Corporation

The continuous shrinking of CMOS device node have put stringent requirement on reducing plasma induced damage and under layer film loss during dry etch. It is always almost the case that when a film is etched in a plasma the under layer film sustains some extent of damage and in some cases this film is etched leading to recess. Up until now this was within the noise to some extent, but beyond 22nm technology node this will be critical in defining device performance. Si roughness and recess during FEOL etch (like gate and spacer) results in degradation of device performance; like shift in threshold voltage, high leakage current leading to increased power consumption. These are some of the roadblocks in achieving high device performance at high packing density. Therefore, it is desirable to attain infinite selectivity between the film that is intended to be etched and its underlying film such that the under-layer film is damage free. In many cases strategies to control Si damage leads to tradeoffs like tapered profile which is not acceptable. This talk will discuss some of the issues in controlling Si damage in FEOL applications and some interesting results.

2:40pm **PS1-MoA3 Structural and Electrical Characterization of HBr/O_2 Plasma Damage to Si Substrate**, ***M. Fukasawa***, Sony Corporation, Japan, *Y. Nakakubo, A. Matsuda, Y. Takao, K. Eriguchi, K. Ono,* Kyoto University, Japan, *M. Minami, F. Uesawa,* Sony Corporation, *T. Tatsumi,* Sony Corporation, Japan

Suppression of Si substrate damage caused by energetic ion bombardment is one of the most critical issues in advanced devices. Si substrate damage during gate electrode etching causes the "Si recess" structure, which is reported to degrade device performance. In previous work, we developed a bilayer model (surface oxide/dislocated Si) of the damaged layer and studied monitoring methods. In this paper, we have investigated the damage generation by plasma exposure and the removal of damage by wet treatment. We have also studied the impact of the damage on electrical performance. A dual frequency (60/13.56 MHz) CCP reactor was used in this study. A SiO_2 layer (1.7 nm) was formed on the Si substrate and exposed to HBr/O_2, H_2, and O_2 plasma. The pressure and Vpp were kept constant at 60 mTorr and 420 V. Diluted HF (100:1) was used to perform a wet treatment. The Si substrate damage was analyzed by spectroscopic ellipsometry (SE), HRBS, and TEM. In the SE analysis, data was fitted using a four-layer model (ambient/SiO_2/dislocated Si/substrate). Dislocated Si was modeled as a mixing of SiO_2 and polysilicon. C-V characteristics were measured with a mercury probe system. HBr/O_2 plasma generates a thicker surface oxide layer than O_2 plasma. The root cause of the thick oxide layer is enhanced diffusion of oxygen in the dislocated Si layer generated by deep penetration of H^+ from the plasma. The thickness of the oxide layer (T_{ox}) increased monotonically with increased exposure time (t) and reached about 10 nm at 600 s. The T_{ox} was found to depend on $t^{1/2}$, which is a so-called parabolic relationship (diffusion-controlled oxidation) in the Deal-Grove model. The T_{ox} and the thickness of the underlying dislocated Si layer (T_d) were compared by SE, HRBS, and TEM. The results were quite consistent across all analyses. The T_{ox} and T_d after dHF treatment were also analyzed. The surface SiO_2 was completely removed and the upper part of the dislocated Si was also eliminated (generation of Si recess). As the remaining dislocated Si was mainly caused by H^+ ion penetration, the C-V characteristics for H_2 plasma-exposed samples were analyzed. A negative bias voltage shift was observed, which implies the generation of positive charge trapping in the interface between the surface oxide and the dislocated Si layer. To minimize the Si damage during gate etching, it is necessary to control the H^+ penetration depth within the thickness of the thin gate oxide by controlling the IEDF precisely. Thus, quantitative control of the IEDF, precise monitoring of surface structure, and understanding the effects on device performances are indispensable for creating advanced devices.

3:40pm **PS1-MoA6 FEOL Etch Challenges for Beyond 2x Technology Node: What does it mean for Energy Consumption?**, ***C. Lee***, *M. Davis, V. Vahedi*, Lam Research Corporation **INVITED**

Energy reduction has become an emerging trend for semiconductor equipment manufacturing; as the technology evolves, demands for higher throughput on the etching of high aspect ratio structures (as driven by DRAM and NAND devices) have placed more demands on the amount of RF power required. A direct consequence of this is more energy is required, both to drive the RF generators and to provide the cooling necessary in order to remove heat generated. This talk will provide an overview on direct energy resource usage, such as power, water, thermal load, process gas usage, and what role does each of these play in the beyond 2x technology node.

4:20pm **PS1-MoA8 Advanced Gate Patterning of Novel Multi-Gated Devices for 15nm Node and Beyond**, ***S.U. Engelmann***, *Y. Zhang, M.A. Guillorn, S. Bangsaruntip, N.C. Fuller, W.S. Graham, E.M. Sikorski*, IBM T.J. Watson Research Center

To continue scaling CMOS devices at the traditional pace following Moore 's law, Short Channel Effects (SCE) are the major issues limiting the use of planar device geometries for future technology nodes. Alternative device integration schemes are currently being tested to test the impact on SCE and extend technology nodes even further. The device candidates that are currently being tested include planar devices, FinFETs, Trigates and Nanowires (gate all around device). The gate formation on these advanced, multi-gated devices imposes completely new challenges on the plasma etch conditions, which translates to the demand to control the plasma process in a second (and a third) dimension. E-beam lithography has been proven to be a very valuable tool to explore plasma processing at device sizes unattainable by state-of the art optical lithography. We have demonstrated the fabrication of gates above a Fin of varying dimensions of gate and fin for SRAM cells down to $0.025um^2$. Significant challenges for this

integration lie in the gate as well as the spacer formation, while maintaining the Si fin that has no hardmask to prevent plasma damage. While maintaining a vertical gate profile, no Silicon loss was observed on the Si Fin. A more significant challenge is the spacer formation, where Nitride needs to be removed from the fin sidewall, while maintaining it on the gate sidewall to prevent device shorts. An even higher degree of process control is needed in the fabrication of nanowire or gate all around devices. Maintaining a vertical gate profile while not damaging or destroying nanowires of diameters less than 5nm is critical. A gate recess process was employed to release the nanowire structures. A highly selective spacer rie process was developed to yield nanowires down to 3nm in diameter.

4:40pm **PS1-MoA9 Plasma Etching Challenges for Patterning Advanced Gate Stacks for 22nm Node and Beyond**, ***Y. Zhang***, *S.U. Engelmann, Q. Yang, R.M. Martin, E.A. Joseph, M.A. Guillorn, E.M. Sikorski, W.S. Graham, B.N. To, N.C. Fuller*, IBM T.J. Watson Research Center

There are increasingly more challenges facing by patterning advanced gate stacks due to continuously scaling of CMOS device dimensions to 22 nm node and beyond. The major causes are from the following: (1) new materials being introduced for advanced gate stacks to enable continuously scaling of T_{inv}; (2) continuously shrinking of pitch and higher density; (3) complex gate patterning integration schemes, such as double or multiply exposures and double or multiply etching with multiply layer mask schemes due to the delay of EUVL; (4) 3D active area and gate structures, such as finFET, tri-gate, Si nanowire (SiNW) FET, etc.; and (5) move to the deep-nanometer regime, such as ETSOI with < 5nm Si channel. The 3D structures with the combination of novel materials and sub-50nm pitches for gate stacks impost unique challenges and demands on plasma etch process technology and news integration schemes and plasma etch tooling innovations. To meet all the requirements of target pitches, device feature profile, line edge roughness (LER) or line width roughness (LWR), and device performance/functionality, Different and unconventional approaches have to be introduced in plasma etching processing to fabricate 3D fins/active area, gates and spacers, particularly with the use of metal/high-k dielectric gate stack materials. Recent results illustrating some of these etching challenges including the progresses developed aiming on improving 3D profiles and achieving increased control of LER/LWR for fin, gate and spacer structures will be presented.

5:00pm **PS1-MoA10 High Selectivity SiN Etching with Low Damage by RLSA Microwave Plasma**, ***M. Inoue***, *M. Sasaki, Y. Ohsawa*, Tokyo Electron, LTD., Japan

New materials such as High-K/Metal Gate and three-dimensional structures such as Tri-Gate have been introduced at the 22nm node and beyond. In addition, high selectivity and reduced Plasma Induced Damage (ex. Charge up damage and Si crystal damage, etc.) are required of the etching process. Especially, Fin Spacer of Tri-Gate is required high selectivity to thin oxide. RLSA (Radial Line Slot Antenna) microwave plasma has several features that overcome these new challenges. The characteristics of RLSA plasmas include high density, low electron temperatures and low plasma potential. In addition, Radical/ion ratio is higher than conventional plasma source. These characteristics enable highly selective etching with decreased Plasma Induced Damage on the wafer surface. A high SiN/SiO selectivity process has been achieved due to the features of RLSA plasma and low bias (low Vpp) conditions.

We have recently developed a high selective SiN/Si etching process under low bias conditions. It is thought that the mechanism for this etch includes minimum oxidation (native oxide level) of the Si surface to SiO, creating a highly selective etch similar to the SiN/SiO process that was previously developed.

5:20pm **PS1-MoA11 Impact of Plasma and Annealing Treatments on 193nm Photoresist Line Width Roughness and Profile**, ***L. Azarnouche***, STMicroelectronics, France, *E. Pargon, K. Menguelti, M. Fouchier,* Ltm - Umr 5129 Cnrs, France, *R. Tiron,* CEA-LETI-MINATEC, France, *P. Gouraud, C. Verove,* STMicroelectronics, France, *O. Joubert*, Ltm - Umr 5129 Cnrs, France

As the Critical Dimension (CD) of gate transistors scales down to the nanometer range, line width roughness (LWR) becomes a serious issue, which directly impacts the electrical performance of CMOS devices. It has previously been shown that the photoresist (PR) sidewall roughness present after lithography (6nm, 3σ) is transferred during the subsequent plasma etching processes into the gate, resulting in a final LWR far above the ITRS requirements for the 32nm technological node (1.7nm, 3σ). The key to decrease the final gate LWR is to minimize the photoresist LWR before the plasma etching steps involved in the gate patterning process. The best and simplest way is to expose the photoresist patterns to plasma treatments prior to gate patterning. Indeed, it was observed that Vacuum Ultra Violet (VUV) light emitted by plasmas plays a key role in the photoresist LWR decrease. In the present study, we have used CD-SEM and CD-AFM techniques to investigate the impact of plasma treatment on the photoresist LWR and profiles. Several plasmas (HBr, Ar, He, H_2) emitting strongly in the VUV region (100-200nm) have been investigated. LiF windows placed between the plasma and the photoresist patterns have been used to evaluate the role of the plasma VUV light only on the LWR evolution. The role of the substrate temperature has also been studied. Many characterization techniques have been used to characterize the physico-chemical modifications of photoresist films exposed to the same plasma treatments (Multiple Internal Reflection infrared spectroscopy (MIR), Raman, gas chromatography (GC)).

The results obtained indicate that all plasma treatments lead to a LWR decrease. We have observed that for all plasma investigated, VUV light only seems to induce a slight reflow of the resist which is probably correlated with the LWR decrease. On the other hand, in HBr and Ar plasmas, resist patterns remain square indicating that no reflow occurs. Heating resist patterns up to 200°C without plasma exposure also leads to a LWR decrease, resist reflow being only observed above 200°C . All treatments generate the cleavage of the side groups (lactone group for plasma treatment and protecting group for annealing treatment) and the decrease of the glass transition temperature which is potentially correlated to the LWR decrease. GC analysis also reveals that under Ar and HBr plasma exposure, cleaved side groups can be trapped in the resist polymer matrix because of the presence of a denser surface layer. This dense layer could prevent the resist reflow leading in final to the square profiles observed in HBr plasmas.

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