Wednesday Afternoon, October 20, 2010

Electronic Materials and Processing
Room: Dona Ana - Session EM+SS-WeA

High-k Dielectrics for III-V Electronics

Moderator: A.C. Kummel, University of California at San Diego

2:00pm **EM+SS-WeA1 High-k III-V MOSFETs Enabled by Atomic Layer Deposition**, ***P. Ye***, Purdue University **INVITED**

The principal obstacle to III-V compound semiconductors rivaling or exceeding the properties of Si electronics has been the lack of high-quality, thermodynamically stable insulators on III-V materials. For more than four decades, the research community has searched for suitable III-V compound semiconductor gate dielectrics or passivation layers. The literature testifies to the extent of this effort. The research on ALD approach is of particular interest, since the Si industry is getting familiar with ALD Hf-based dielectrics and this approach has the potential to become a manufacturable technology.

Using In-rich InGaAs as surface channel, high-performance inversion-mode high-k/III-V NMOSFETs have been demonstrated. By further improving on-state performance, such as maximum drain current I_{dss} and peak transconductance G_m, the off-state performance or subthreshold characteristics need to be seriously evaluated for digital applications. In this talk, we review some new progresses on deep-submicron inversion-mode $In_{0.7}Ga_{0.3}As$ NMOSFETs using 2.5 nm-5.0 nm ALD Al_2O_3 as high-k gate dielectrics. The G_m exceeds 1.1-1.3 mS/μm and starts to approach the values from InGaAs HEMTs. The scaling metrics, such as threshold voltage (V_T), I_{on}/I_{off} ratio, sub-threshold swing (*S.S.*), the drain induced barrier lowing (*DIBL*), as a function of the gate length from 150 nm to 250 nm are systematically studied. Retro-grade structure and halo-implantation are also applied to III-V MOSFET field to improve the off-state performance of InGaAs MOSFETs.In order to achieve better gate control capability, new structure design like FinFET demonstrated successfully in Si devices, is strongly needed for short-channel III-V MOSFETs. However, unlike Si, the dry etching of III-V semiconductor surface has been believed to be difficult and uncontrollable, especially related with surface damage and integration with high-k dielectrics. We also review some results on the first experimental demonstration of inversion-mode $In_{0.53}Ga_{0.37}As$ tri-gate FinFET using damage-free etching and ALD Al_2O_3 as gate dielectric. The SCE is greatly suppressed.

The work is in close collaborations with Y.Q. Wu, Y. Xuan, J.J. Gu and M. Xu. We also would like to thank valuable discussions with D. Antoniadis, M.S. Lundstrom, R.M. Wallace, K.K. Ng, M. Hong, and J. Woodall.

2:40pm **EM+SS-WeA3 Passivation of Al_2O_3/InGaAs(100) Interfaces by Atomic Layer Deposition and Annealing**, ***F.L. Lie***, *B. Imangholi*, University of Arizona, *W. Rachmady,* Intel Corp., *A.J. Muscat*, University of Arizona

Identification of the source of interfacial defects between high-k films and III-V substrates is crucial for developing passivation methods. Efforts have been made to isolate defects based on a specific chemical moiety at an interface. A study reported that doubly-O coordinated Ga and displaced As formed when GaAs is exposed to oxygen, induces mid-gap states[1]. Another study suggested that high activity interface defects originate from structural disorder instead of specific chemical moieties[2]. This project aims to understand the nature of Al_2O_3/InGaAs interface defects by relating composition to electrical performance. The modification of InGaAs(100) surfaces due to surface cleaning, Al_2O_3 deposition, and post deposition annealing (PDA) was investigated using capacitance-voltage (CV) curves, large AC signal conductance (LSC), and x-ray photoelectron spectroscopy (XPS). Al_2O_3 films were deposited by atomic layer deposition (ALD) using trimethylaluminum (TMA) and water precursors on native oxide covered and aqueous HF etched InGaAs(100) surfaces. XPS analysis on a native oxide sample revealed ~8Å oxide (52% As, 29% Ga, and 21% In) and a monolayer excess of As on an As-terminated substrate. TMA reacted on this surface during ALD, thinning the oxide to ~4.2 Å (45% As, 29% Ga, and 27% In). Aqueous HF treatment removed the native oxide and produced an As-rich surface, which re-oxidized in air. Surfaces consisted of ~4.2 Å oxide (91% As) and 1.5 monolayer excess As on an As-terminated surface. ALD Al_2O_3 on the liquid-cleaned surface produced a chemically sharp Al_2O_3/InGaAs interface with less than a monolayer of As oxide. CV and LSC measurements were performed on Au/Ni/10 nm Al_2O_3/InGaAs stacks. The deep-level surface recombination velocity (SRV) values extracted represent the net effect of interface defects, which includes the defect density and capture cross section. The similar SRV values obtained for native oxide (34±6 cm/s) and aqueous HF (29±13 cm/s) prepared surfaces suggest that the presence or absence of oxides was not the only determining factor. PDA in forming gas and NH_3 ambients significantly improved the electrical quality, as reflected in SRV values of 1 to 5 cm/s for both surfaces. XPS analysis showed increased excess As and Ga_2O_3 at the interface of both surfaces, likely due to thermally or H-induced reactions between interfacial As oxide and Ga atoms in the substrate. These results suggest that high activity defects in III-V's could be associated with interfacial dangling bonds and are amenable to standard passivation methods used in Si technology.

[1]Hale M. J. et al, J. Chem. Phys. 119(13), 2003

[2]Caymax M. et al, Microelectron. Eng. 86, 2009

3:00pm **EM+SS-WeA4 An In Situ Examination of Atomic Layer Deposited Al_2O_3/InAs(100) Interfaces**, ***A.P. Kirk***, *M. Milojevic, D.M. Zhernokletov, J. Kim, R.M. Wallace*, University of Texas, Dallas

An in situ half-cycle atomic layer deposition/X-ray photoelectron spectroscopy (ALD/XPS) procedure was conducted in order to learn more about the evolution of the Al_2O_3 dielectric interface with undoped InAs(100). Without breaking vacuum, monochromatic XPS was used to examine the InAs(100) surface following ammonium sulfide passivation or ammonium hydroxide etching and then after each individual ALD pulse of trimethyl aluminum (TMA) and deionized water (DIW) precursors (e.g. single TMA pulse/XPS scan; single DIW/XPS scan; etc.). Ammonium sulfide was more effective at minimizing native oxides than ammonium hydroxide. Regardless of chemical cleaning technique, after depositing up to 1 nm of Al_2O_3, elemental arsenic (As^o or As-As bonds) remained at the interface which may have adverse implications for devices such as metal oxide semiconductor field effect transistors (MOSFET). After heating to 300 °C (typical ALD reactor temperature), As-S bonding was reduced below the XPS detection limit. The In^{1+} chemical state (e.g. In_2O) was preserved while trivalent In and As oxidation states were minimized following exposure to TMA. The chemical reaction pathways appear to be similar to that observed for GaAs and InGaAs. We will also present electrical characterization studies and examine the correlation to the in situ interface analysis.

4:00pm **EM+SS-WeA7 Fermi-level Unpinning of HfO_2/$In_{0.53}Ga_{0.47}As$ Gate Stacks using Hydrogen Anneals**, ***R. Engel-Herbert***, *Y. Hwang, N.G. Rudawski, S. Stemmer*, University of California, Santa Barbara

Compound (III-V) semiconductors are currently being investigated to replace Si as channel material in metal oxide semiconductor field effect transistors. A significant challenge is the high trap density (D_{it}) at the dielectric/III-V semiconductor interface, causing Fermi level pinning. Recently, it has been reported that the D_{it} can be reduced by sulfur passivation and hydrogen annealing for Al_2O_3/$In_{0.53}Ga_{0.47}As$ interfaces.

In this presentation, we will present our studies of the effect of forming gas anneals on the electrical properties of HfO_2/$In_{0.53}Ga_{0.47}As$ metal oxide semiconductor capacitors . HfO_2 films with thicknesses between 9 and 18 nm were deposited in-situ on As-decapped n-type $In_{0.53}Ga_{0.47}As$ channels by chemical beam deposition using hafnium *tert*-butoxide (HTB) as the source. Samples were post-deposition annealed in forming gas. For comparison samples annealed in nitrogen were also studied. Capacitance-voltage (CV) and conductance-voltage (GV) curves were measured at room temperature. The interface trap density D_{it} was quantified using both the Terman and the conductance methods. The conductance method showed that the D_{it} was reduced from $1.3X10^{13}cm^{-2}eV^{-1}$ to $8X10^{12}cm^{-2}eV^{-1}$ near midgap. The conductance peak shifted in frequency with a change in negative gate voltage, consistent with an unpinned Fermi level. The 1 MHz CV curve reached the calculated minimum capacitance value, indicating Fermi level unpinning. The nitrogen annealed control sample did not reach the minimum capacitance and the conductance peak shift at negative bias was moderate, indicating Fermi level pinning at midgap. We will also present comparisons of the extracted band bending for both nitrogen and forming gas annealed stacks and discuss the mechanisms by which forming gas anneals can reduce the midgap D_{it}.

4:20pm **EM+SS-WeA8 Valence Band Alignment in low-k Dielectric/Cu Interconnects as Determined by X-ray Photoelectron Spectroscopy**, ***S. King***, *M. French, M. Jaehnig, M. Kuhn*, Intel Corp.

Electrical leakage in low-k/Cu interconnect structures is becoming a growing vital concern as the nano-electronics industry moves to increasingly tighter metal spacing's for sub 22 nm technology nodes and continues to replace dense SiO2 dielectrics with low density / porous SiOC:H "low-k" dielectric materials. In order to understand the various possible leakage mechanisms in low-k/Cu interconnects, a knowledge of the

basic band alignment between Cu and low-k dielectric materials is needed but has gone largely unreported. In this regard, we have utilized X-ray Photoelectron Spectroscopy (XPS) to measure the Valence Band Alignment and Schottky Barrier at interfaces of importance to Cu/low-k interconnects. XPS has been used extensively for determining the band alignment of numerous semiconductors to other semiconductors, metals, and dielectrics. In this paper, we demonstrate that XPS can also be utilized to determine the band alignment at interfaces between amorphous dielectrics and metals of interest to the low-k/Cu interconnects industry. Specifically, we have utilized XPS to determine the Schottky Barrier between Cu and low-k dielectric SiC and SiCN capping layers deposited on Cu via Plasma Enhanced Chemical Vapor Deposition (PECVD). We have also utilized XPS to determine the valence band alignment at SiCN:H/SiOC:H interfaces. Lastly, the impact of various plasma surface treatments on the band alignment at these interfaces was also investigated.

4:40pm **EM+SS-WeA9 III-V CMOS: A sub-10 nm Electronics Technology?**, ***J.A. del Alamo***, Massachusetts Institute of Technology **INVITED**

CMOS scaling is at the heart of the microelectronics revolution. The ability of Si CMOS to continue to scale down transistor size while delivering enhanced performance is becoming increasingly difficult with every generation of technology. For Moore's law to reach beyond the limits of Si, a new channel material with a high carrier velocity is required. A promising family of materials for this is III-V compound semiconductors.

III-Vs are well known for their unique suitability for high frequency electronics. III-V-based integrated circuits are currently in use in a variety of communications and defense applications. The prospect of III-Vs entering the logic roadmap is tantalizing. This work reviews some of the critical issues.

The barrier for insertion of a new channel material into the CMOS roadmap is huge. Any new technology has to beat Si designs in performance at device footprints that allow the integration of billions of transistors on the same chip. In addition, cost-effective manufacturing must be realized.

To make this work, a III-V CMOS technology has to solve a number of challenging technical problems. The development of a gate stack that includes a high-K dielectric and yields a high-quality semiconductor interface with a III-V compound semiconductor is up there as one of the greatest and most fascinating problems in modern semiconductor technology. Recent research suggests that this is an eminently attainable goal. Transistor size scalability is also a major worry. Will it be possible to scale future III-V transistors to the required dimensions while preventing excessive short-channel effects and attaining the demanding parasitic resistance objective? This is a topic that will call for extensive experimental and simulation research. Fortunately, calibrated simulators today reproduce quite well the characteristics of 30 nm gate length III-V FETs and should be valuable in projecting to devices in the 10 nm range. If planar device designs are unsuitable, 3D designs might offer a viable path. Recent 3D device demonstrations with impressive characteristics give hope that this is a promising strategy. A future III-V CMOS technology will also have to "look and feel" as much as Si as possible. This calls for the formation of thin high-quality III-V layers on top of large Si wafers. In fact, depending on what emerges as the best option for the p-channel device, a major challenge in itself, two dissimilar materials might need to be integrated side by side in very close proximity on top of a Si wafer. These are all great problems that will require the coordinated attention of scientists and technologists with expertise in many different domains.

5:20pm **EM+SS-WeA11** , ***W. Melitz***, *J. Shen, S. Lee, J.S. Lee, A.C. Kummel*, University of California at San Diego, *S. Bentley, D. Macintyre, M. Holland, I. Thayne*, University of Glasgow, UK

Cross-sectional scanning probe microscopy (SPM) is an imaging technique which can map the potentials inside an operational MOSCAP or MOSFET device. Kelvin probe force microscopy (KPFM) measures the contact potential difference (CPD) of a conductive cantilever and a sample surface with a precision of better than 10 meV. In cross-sectional KPFM, (X-KPFM) a fully functional MOSFET or MOSCAP is cleaved in UHV, and the potential inside the working device is measured in two-dimensions; UHV cleaving is critical to preserve an oxide-free surface so the unperturbed potentials can be measured. Cross-sectional KPFM can determine the effect of surface passivation of the gate oxide in operational devices, influence of the fixed charge in the gate oxide with semiconductor channel material, structural features and their effects on the potential distribution, and even work function offsets of the gate and semiconductor. The biggest challenges in imaging cleaved devices is obtaining good cleaves and finding the structure of interest while maintaining good tip conditions for high resolution. Using a comb structure for the electrodes increases the density of the devices on the cleave face to increase the number of working devices. The cleave edge of the sample drastically affects the stability of the cantilever. In order to increase the stability, the devices were embedded in a >300nm insulator; therefore, the device of interest in not located directly on the edge face. Using this capping technique, high spatial resolution in a UHV cleaved MOSCAP with KPFM shows the amount of band bending in the semiconductor channel caused by the fixed charge in the oxide. High resolution KPFM has also been demonstrated for a range of external gate biases, illustrating the flexibility of KPFM for investigating MOS devices. Current efforts focus on implementing KPFM into patterned scaled MOSCAP and MOSFET devices.

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