Plasma Science and Technology
Room: B2 - Session PS2+MN-WeA

High Aspect Ratio and Deep Etching for 3D Integration and Memory
Moderator: S. Hamaguchi, Osaka University, Japan

2:00pm **PS2+MN-WeA1 Advanced DRIE Via Etching**, ***F. Gao**, D. James, K. Kolari, J. Kiihamäki,* VTT Technical Research Centre of Finland, *M. Muggeridge*, Aviza Technology, Inc.

We present 3 different types of interconnection vias fabricated by deep reactive ion etching (DRIE) on silicon substrates. One type of vertical vias with 30µm diameter mask opening are etched through 400µm thick wafer by switched Bosch process, featured by very fast etch rate at about 6µm/min and over 12:1 aspect ratio. The other type of vertical vias are tested on smaller diameters ranging from 1-9µm and etched to 20-50µm deep. Those vias have the minimum undercut and smooth sidewalls achieved by non-switched etching. Another type of tapered vias with 75µm mask opening are etched isotropically in DRIE resulting in over 150µm deep vias with 70-80 degree tapering. Silicon etch selectivity against different mask materials are studied and compared for the vertical vias. Thick resist is thought to be better mask to minimize undercut and via top erosion by reflected ions. Tapered vias have the problem of sidewall roughness from the isotropic etch. Both plasma cleaning and argon annealing methods are tested to smooth the silicon sidewalls in the tapered vias.

2:20pm **PS2+MN-WeA2 The Generation and Removal of Heat during DRIE of High Aspect Ratio Structures in SOI with Buried Cavities**, ***J. Dekker**, F. Gao, J. Kyynäräinen, J. Kiihamäki*, VTT Microelectronics Research Center of Finland

This work examines the accumulation of heat and resulting increase in local temperature and loss of selectivity which may occur when etching high aspect ratio structures in SOI wafers with buried cavities. It is shown that unlike high-load, high-rate etches treated elsewhere, in the case of HAR etches the heat is generated mainly by ion-bombardment. Due to the presence of a cavity beneath the structures being released, which typically include a mass suspended by springs, the heat may only be conducted laterally away from the released structures to the surrounding device layer. During the final stages of DRIE etch and overetch, the heat flow from suspended masses is therefore restricted to occur along the springs which attach the mass to the surrounding device layer. The limited heat conductance of long meander springs in particular is unable to remove the heat generated in suspended structures. As a result, the temperature of the suspended structures increases resulting in reduced fluorocarbon depositon upon them. That, in turn, results in a locally increased etch rate of the oxide mask on the suspended structures. The effects of releasable thermal anchors, which provide additional paths for heat conduction away from the suspended mass and therefore aid in the removal of heat, is also discussed.

2:40pm **PS2+MN-WeA3 Ion Trajectory Prediction at High-Aspect-Ratio Hole Etching by the Combination of On-Wafer Monitoring and Sheath Modeling**, ***H. Ohtake**, S. Fukuda, B. Jinnai,* Tohoku University, Japan, *T. Tatsumi,* OKI Semiconductor Miyagi Co., Ltd., Japan, *S. Samukawa*, Tohoku University, Japan

The abnormal etching profiles, such as bowing, etch stop and twisting, have been reported at high-aspect-ratio hole etching. To avoid the failures, we have to predict the ion trajectory and etching profile precisely by analyzing the sheath area around the hole. In this presentation, we developed the ion-trajectory prediction system at high-aspect-ratio hole by combining the on-wafer monitoring technique and sheath modeling for explaining and predicting the etch stop and twisting. Since our developed on-wafer sensors provide the surface potential, the electron density/ temperature and side-wall resistance of the hole, we can simulate the distribution of electric field in the hole. This system revealed that the sidewall conductivity strongly affects the charge-up and ion trajectory in the high-aspect-ratio hole. It also predict the etch stop and twisting phenomena. Consequently, we believe this prediction system is an effective tool for developing the nano-scaled fabrication.

3:00pm **PS2+MN-WeA4 Enhancement Mechanism of Distortion and Twisting in Ultra High Aspect Ratio Dielectric Etching**, ***H. Mochiki,*** Tokyo Electron AT Ltd., Japan, *K. Yatsuda,* Tokyo Electron Ltd., Japan, *S. Okamoto, F. Inoue*, Tokyo Electron AT Ltd., Japan

It is required to fabricate capacitors with aspect ratio of from 40:1 to 60:1 for DRAM at hp 3x nm and beyond generation, and etching such ultra high aspect cylindrical shapes without distortion and/or twisting is the most difficult challenge. Recently, it has been reported that distortion and twisting were caused by electron shading effects, electrical potential difference between the top and bottom of dielectric during plasma etching. In this paper, we report how distortion and twisting are enhanced, and how they can be minimized.

First of all, electron shading effects are results of electrostatic charge on the surface of etched dielectric material – silicon dioxide, and organic capacitor mask is negatively charged where silicon dioxide surface is positively charged. At these generations, DRAM devices are so largely scaled that their capacitors need to be fabricated very close to each other. Consequently, incident positively charged ions in a cylinder, accelerated by plasma sheath, receive repulsive force from not only the cylinder surface itself but also neighboring cylinder surfaces. We confirmed that grad of distortion and twisting changed by altering the layout of capacitors.

On the other hand, we found that distortion and twisting could also be generated from the very beginning of etching at the low aspect ratio portion by observing the top view of a cylinder every 100 nm-deep from the wafer surface. Moreover, we affirmed that distortion strongly correlated with capacitor etch mask profile when varying it on purpose by changing mask etch conditions. Thus, we clarified that another enhancement mechanism of distortion existed apart from electron shading effects.

Therefore, there are several enhancement mechanisms of distortion and twisting, and it is necessary to address each solution. We divided the enhancement mechanisms of distortion and twisting into two modes, which are generated at low and high aspect ratio, and examined their solutions from the etching point of view, respectively. We conclude that the optimization of capacitor etch mask profile was the most effective solution at the low aspect ratio mode, and higher dissociation plasma with relatively higher plasma density and superimposed DC on CCP (capacitively coupled plasma) improved distortion and twisting at the high aspect ratio mode.

4:00pm **PS2+MN-WeA7 High Rate Deep Si Etching for TSV Applications**, ***I. Sakai**, N. Sakurai, T. Ohiwa*, Toshiba Corporation, Japan **INVITED**

Si etch process for etching deep and high-aspect ratio structures has been studied intensely for applications such as DRAM trench capacitors and MEMS devices. Recently, there is focus on Si etching for TSV (through Si via) applications for 3-D (three-dimensional) LSIs. Dimensions of the TSVs which are being investigated today vary widely, depending on its application and integration scheme. For example, TSV for 3-D packaging of logic devices may be sub-micron to a few microns in diameter and about 10 microns deep. On the other hand, TSVs used in stacking memory devices, the via diameter and depth would be several tens of microns, and, package for CMOS image sensors using TSVs may have via diameters and depths up to 100 microns.

For TSVs up to 10 microns in depth, the conventional Si deep trench etch process for DRAMs can be easily adapted to etching TSVs because of its similar dimensions. The typical etch rate is several microns per minute. On the contrary, etching of very deep holes of depths on the order of tens of microns and up to 100 microns is not within the experience of conventional front-end LSI fabrication processes. In this case, consequently, an extremely high Si etch rate becomes mandatory because of cost issues, especially for TSV applications which require via holes more than 20 microns deep.

To fulfill this requirement for TSV applications, the Si etch process was investigated focusing on the Si etch rate. First, a large via size of 40 microns was studied, and an etch rate of more than 50 µm/min was realized. It was found that the Si etch rate depended on fluorine radical density, so, high rate was obtained by creating a high fluorine radical density condition by using a high pressure condition of 350 mTorr, with a capacitively-coupled plasma (CCP) reactor with a Dipole-Ring Magnet (DRM) and SF_6 gas chemistry. Furthermore, the etch process for smaller holes of 8 microns was studied to realize high etch rates also. The etch process was modified to obtain a straight etch profile, then, via holes were etched to a depth of 60 microns at an etch rate of 24 µm/min.

High rate deep Si etching is realized for TSV application for holes more than 20 microns deep, using CCP RIE with SF_6–based gas chemistry.

4:40pm **PS2+MN-WeA9 Infinitely High Etch Selectivity and Variation of Line Edge Roughness during Etching of Hard-Mask Layer with Patterned Extreme Ultra-Violet**, ***B.S. Kwon***, *J.S. Kim, C.R. Jung, J.S. Park, W. Heo, N.-E. Lee,* Sungkyunkwan University, Korea, *S.K. Lee*, Hynix Semiconductor, Republic of Korea

In the nano-scale Si processing, patterning processes based on multilevel resist structures becoming more critical due to continuously decreasing resist thickness and feature size. In particular, highly selective etching of the first dielectric layer with resist patterns and control of critical dimension (CD) and ling edge roughness (LER) are of great importance. In this work, process window for the infinitely high etch selectivity of silicon oxynitride (SiON) layers to EUV resist and variation of LER of extreme ultra-violet (EUV) resist was investigated during etching of SiON/EUV resist in a $CH_2F_2/N_2/Ar$ and $CH_2F_2/N_2/O_2/Ar$ dual-frequency superimposed capacitive coupled plasma (DFS-CCP) by varying the process parameters, such as the CH_2F_2 and N_2 flow ratio, low-frequency source power (P_{LF}) and O_2 flow rate. It was found that the CH_2F_2/N_2 flow ratio was found to play a critical role in determining the process window for infinite SiON/EUV resist etch selectivity, due to the differences in change of the degree of polymerization on SiON and EUV resist. Control of N_2 flow ratio gave the possibility of obtaining the infinitely high etch selectivity by keeping the steady-state hydrofluorocarbon layer thickness thin on the SiON surface due to effective formation of HCN etch by-products and, in turn, in continuous SiON etching, while the hydrofluorocarbon layer is deposited on the EUV resist surface. On the other hand, CD size and LER tend to increase with increasing CH_2F_2/N_2 flow ratio.

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