Plasma Science and Technology
Room: A1 - Session PS1-TuM

Advanced FEOL and BEOL Etch
Moderator: Y. Kimura, LAM Research

8:00am **PS1-TuM1 Inductively-Coupled Pulsed Plasmas in the Presence of Synchronous Pulsed Substrate Bias for Advanced Gate Etching**, ***S. Banna***, Applied Materials Inc., *K. Tokashiki*, Samsung Elect. Co. Ltd., *A. Agarwal*, Applied Materials Inc., *J.Y. Lee*, Samsung Elect. Co. Ltd., *V. Todorow*, Applied Materials Inc., *J.H. Yoon*, Samsung Elect. Co. Ltd., *S. Rauf*, Applied Materials Inc., *K. Shin*, Samsung Elect. Co. Ltd., *K. Ramaswamy, P.J. Stout, D. Lymberopoulos, K. Collins*, Applied Materials Inc. **INVITED**

The pace at which microelectronics technology is progressing is highly challenging with conventional device architecture. The stringent and conflicting requirements in microelectronics for damage-free plasma etching processes, with improved uniformity, higher selectivity, better anisotropy, more precise ion energies/fluxes control and enhanced process throughput have stimulated an intensive research effort among academic and industrial communities. This research is focused on novel approaches for the design/control of the next generation of plasma processing reactors. Following the above challenges, the dry etch process regime for gate etching has moved towards low pressure plasmas with higher densities. In this regime, the risk of plasma induced damage(PID) or charging damage increases, potentially affecting the overall device electrical performance. PID includes UV damage and highly energetic ion bombardment damage. Moreover, for high aspect ratio structures, electron shading effect becomes more dominant enhancing the risk of charging damage. In the past, it was demonstrated that pulsed radio frequency(PRF) inductively coupled plasmas(ICP) have the promise to address some of the above challenges. Typical commercial ICP reactors consists of 2 RF power supplies, the RF source which is fed to the antenna coils of the ICP source and RF bias applied to the substrate. Accordingly, 3 main different regimes of operation for pulsed plasmas might take place. The first, known as source pulsing, in which the source is operating in PRF mode while having the bias in continuous wave(CW) mode. The second is bias pulsing i.e. source in CW mode while the bias is in PRF mode. The third one is synchronized pulsing, for which both source and bias are pulsed simultaneously at the same frequency and duty cycle.

Recently we have evaluated the impact of synchronized pulsing plasma on gate etch for sub-50nm DRAM applications. The evaluation included basic etching characteristics such as average etch rate, uniformity and selectivity, 35nm gate critical dimension(CD) uniformity and profile control, and plasma induced damage. It was demonstrated that by control of the synchronous pulse parameters extends the plasma operating conditions range aiming to improve processes for finer features. In particular, we have shown gate CD controllability, PID mitigation, and significant reduction in electron shading effect and in the gate leakage current along with improving the electrical performance of the overall device. 2D plasma and feature scale modeling results will be used to illustrate the basic physics of synchronous pulsing, in particular its effect on the ion energy distribution.

8:40am **PS1-TuM3 Synchronously Pulsed Capacitively Coupled Plasma Sources for Dielectric Etching**, ***A. Agarwal***, *P.J. Stout, S. Rauf, K. Collins*, Applied Materials Inc.

Plasma etching processes for microelectronics fabrication at future technological nodes are extremely challenging. The requirements regarding the uniformity (both etch rate and critical dimensions) are also more stringent than ever. One particular challenge in plasma etching of extremely high aspect ratio features (aspect ratio > 40) is minimizing plasma induced damage, both physical and electrical. The via-like features may physically twist/turn due to the stochastic nature of fluxes entering the feature as the size of the opening shrinks.[1] Charge trapped by the polymer on the sidewalls exaggerates this phenomenon. Alternately, charge retention at the bottom of trenches may lead to breakdown as the material stresses under the accumulated charge creating a weak path for the injected current.[2] Pulsed plasma operation has been shown to be a promising approach to improving uniformity while reducing charge damage.[3] Although pulsing of both capacitively and inductively coupled plasma sources has been investigated before, novel pulsing schemes such as synchronous pulsing in multi-frequency capacitively coupled plasmas (CCP) may allow for expanded operating regime for damage-free etching of high aspect ratio features.

In this paper, pulsed and continuous plasma operation of a multiple frequency capacitive coupled plasma reactor in electronegative gas mixtures will be discussed using results from a computational investigation. A 2/3-dimensional plasma equipment model (CRTRS) [4] has been linked to a Monte Carlo feature profile model [5] to assess the consequences of pulsed plasma operation on etching of dielectric features. Results will be discussed for impact of pulse characteristics such as duty cycle, pulse excitation frequency, phase lag between source and bias pulses on dielectric etching in a multi-frequency CCP chamber. Careful tailoring of pulsing at both source and bias frequencies enables negative charge acceleration in the features and helps negate charge buildup. The impact of varying plasma electronegativity at different gas pressures will also be discussed. If strongly electronegative gas mixtures are used, sustaining a steady pulsed plasma can however be complicated as the plasma may not re-ignite after power is turned-off.

[1] A. Agarwal, M.M. Wang, and M.J. Kushner, 54th AVS Symposium 2007.

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[3] S. Banna, et al., 55th AVS Symposium 2008.

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[5] P. Stout, 60th Gaseous Electronics Conference 2007.

9:00am **PS1-TuM4 Highly Selective and Low Damage Etching of TiN / HfO_2 Layer Gate Stack Structure using Neutral Beam Etching and Atomic Layer Etching**, ***B.J. Park***, *J.B. Park, TH. Min, J.K. Yeon, S.K. Kang, W.S. Lim, G.Y. Yeom,* SungKyunKwan University, South Korea, *K.S. Min*, University of Texas, Austin

As the critical dimension of metal-oxide-semiconductor field-effect transistor shrinks less than 45 nm and below, conventional polysilicon gates on ultrathin SiO2 dielectric layers should be replaced by metal gates on high-k dielectric materials. However, the adoption of these new materials imposes new integration problems. Among many integration issues, the etch selectivity of the etched layers (metal electrode or high-k dielectrics) to the under-layers (high-k dielectrics or Si substrate) is one of the most important issues in the patterning of the gate stack structures.

In order to solve these problems, in this study, we applied two step etch process where, the metal gate electrode is selectively etched using a reactive neutral beam against a high-k dielectric layer and then the high-k dielectric layer is removed using atomic layer etching (ALET) for precise etch depth control.

The result showed nearly infinite etch selectivity of TiN/HfO2 using a HBr/Cl2 neutral beam by controlling energy (<100 eV). In addition, an anistropic etch profile and smooth surface roughness (0.109 nm) could be observed using TEM and AFM. For the ALET of HfO2, the monolayer etching condition of 1.2 Å /cycle could be observed using BCl3 ALET and, after the 30 etch cycles, exactly 3.5nm thick HfO2 layer was removed with a low surface roughness and without the change of surface composition. When we compared the properties of MOSFET devices fabricated using conventional RIE processing and those using the neutral beam/atomic layer etching, the improvement of characteristics of NMOSFET and PMOSFET could be observed for the devices fabricated using neutral beam /atomic layer etching.

ACKNOWLEDGMENT

This work supported by the National Program for Tera-Level Nano devices of the Korea Ministry of Education, Science and Technology (MEST) as a 21st Century Frontier Program.

9:20am **PS1-TuM5 Impact of Cure and Trim Processes on the Linewidth Roughness Transfer during Gate Stack Patterning with Amorphous Carbon Mask**, ***L. Azarnouche***, STMicroelectronics, France, *E. Pargon, M. Martin, O. Luere, K. Menguelti*, CNRS/LTM, France, *P. Gouraud, C. Verove,* STMicroelectronics, France, *O. Joubert*, CNRS/LTM, France

With the continuous scaling down of semiconductor device dimensions, the linewidth roughness (LWR) becomes a non negligible parameter that needs to be controlled in the nanometer range for the future technological nodes (1.7nm (3σ) for the 32 nm technological node). In previous studies, we demonstrated that the 193 nm photoresist mask LWR is the main contributor to the final gate LWR. We also observe that the LWR is mainly decreased during the plasma etching steps in which the resist mask is involved (BARC and hard mask etching). Preliminary conclusion is that the photoresist mask is the first vector of LWR decrease during plasma exposure. The resist LWR is therefore the key parameter to sucessfully control the final metal gate LWR in the nanometer range. In the present study, we first evaluate the impact of HBr cure plasma treatment and resist

trimming processes on the resist LWR and second analyze how these plasma etching steps impact the final gate LWR. LWR measurements are performed using the CD-AFM technique much more powerful than commonly used CD-SEM. First results indicate that both resist trimming and plasma cure treatment processes improve the resist LWR and consequently the final gate LWR. We demonstrate that, during cure processes, plasma Vacuum UltraViolet (VUV) light is mainly responsible for the resist LWR decrease while during trim processes, the plasma VUV light combined to the lateral erosion of the resist induced by reactive radicals is identified as the main contributor to the resist LWR decrease.

However, we also show that the sequence of cure and trim processes has a less important impact on the gate LWR than a cure or a trim process only and that the position of the cure treatment in the sequence of plasma etching steps involved in the gate patterning process has some consequences in the final gate LWR. Finally, as the etching mask used to pattern the gate plays a primordial role in the final gate LWR, we compare the impact of two masking strategies: one using amorphous carbon layer as etching mask and the other one a spin on carbon hard mask.

9:40am **PS1-TuM6 Multilayer Mask Etch - CD, CD Bias, and Profile Control using RLSA Plasma Etcher**, ***H. Kintaka***, *T. Mori,* TEL Technology Center, America, LLC USA, *M. Sasaki, T. Nozawa*, Tokyo Electron Technology Development Institute, Inc. Japan

As the design rule of ULSI devices continue to be scaled down, the critical dimension (CD), CD bias, and the mask profile control technique has been needed. As the result of this study, precise CD control of multilayer mask etching was established by RLSA (Radial Line Slot Antenna) microwave plasma source. The multilayer stack which was used for experiments consisted of Photo Resist/SiARC/Organic/SiN/Si-substrate.

The results are: first, zero Iso/Nest bias was accomplished. As result, the same CD bias is obtained kept in both the Iso and Nest pattern with vertical profile. Second, CD Bias is controlled in the range of several +/- nm with same bias of Iso/Nest by adjusting SiARC etching condition. By these characteristics, it is possible to make hard mask CD same as patterned resist CD in any pattern density.

These results are obtained by RLSA micro-wave plasma characteristics. RLSA generates high density plasma just below top dielectric plate, and as the plasma diffuses forward the wafer, its density and electron temperature become lower by diffusion. The etched by-products do not re-dissociate and not deposit on the wafer in the low electron temperature condition. This result shows that this plasma can etch only biased ion direction without side-wall deposition.

These unique characteristic will remove the burden of adjusting the width in the patterning step.

10:40am **PS1-TuM9 Effects of Hydrogen Bombardment during Polysilicon Gate Etching by HBr/O_2 Plasmas**, ***T. Ito***, *K. Karahashi,* Osaka University, Japan, *M. Fukasawa, S. Kobayashi, N. Kuboi, T. Tatsumi,* Sony Corporation, *S. Hamaguchi*, Osaka University, Japan

As the miniaturization of semiconductor devices continues, better control techniques of substrate surface damages as well as a better understanding of the mechanisms of surface modification during plasma processing are required for future semiconductor manufacturing. Especially during etching processes by HBr/O_2 plasmas, which are widely used for etching of poly-silicon gate electrodes, it has been reported that the silicon substrate under a gate oxide film is seriously damaged during the gate electrode etching process. This phenomenon is known as a "Si recess". The goal of the present study is to understand the cause of the Si recess and to propose a technique to minimize it. To understand the mechanism, we have used a multi-beam injection system, which can irradiate surfaces with independently controlled atoms, molecules and ions. In this way, the system enables us to simulate experimentally plasma-surface interactions that take place during plasma etching processes. The multi-beam system consists of three parts, i.e., a mass analyzed ion beam injector, a set of two independently controllable neutral radical/molecular beam injectors, and a reaction chamber in which a sample substrate can be placed. In this system, a monochromatic and mono-energetic ion beam as well as independently controlled radical/molecular beams can be simultaneously injected into a given substrate surface. The ion and radical sources are differentially pumped and therefore the chamber can be maintained at ultra-high vacuum. The change in chemical nature of the substrate surface can be observed *in situ* by X-ray photoelectron spectroscopy (XPS) that is installed in the reaction chamber. In this study, Si(100) surfaces were irradiated by H^+, Ar^+, or O^+ ion beam at 500eV each as well as atomic oxygen (O) radical beams and are analyzed with (*ex situ*) High-Resolution Rutherford Backscattering (HRBS). The results have shown that a layer of structure alteration with 10 nm thickness is formed on the Si substrate surface only when H^+ ions are injected into the surface. Furthermore it has been found that oxygen (O) diffusion is enhanced in the alteration layer due to amorphization of Si. Thus our multi-beam injection experiments corroborates the hypothesis that the Si recess during HBr/O_2 plasma etching processes is caused by H^+ ion injections from HBr plasmas and O radical diffusion. This also suggests the importance of precise control of incident ion energies for the minimization of Si recesses during the processes.

11:00am **PS1-TuM10 Challenges in Etching sub-45nm Shallow Trench Isolation (STI)**, ***A. Paterson***, *T. Panagopoulos, S. Sriraman, A. Sato, N. Benjamin, N. Williams, C. Lee, Y. Yamaguchi-Adams, A. Eppler, L. Braly, T. Kim, H. Singh, V. Vahedi*, Lam Research

The continued scaling in semiconductor industry provides new challenges for etching Shallow Trench Isolation (STI) features to create active area islands. Control of the STI profile is of primary importance, e.g. trench angle control of $88^o \pm 0.2^o$ being requested across a 300 mm wafer, along with the additional demand to control the trench depth range non-uniformity to <2.5%, for ~2500-3000 Å trench depth. Typically, the stringent profile control requirements are met by operating halogen based Transformer Coupled Plasma (TCP™) plasmas in the mid-pressure operating regime, 20mT to 60mT. However, in this regime the trench depth non-uniformity is upward of 5% and has a characteristic wafer pattern that resembles a "donut", which is due to the electron mean free path, $\lambda_{mfp,}$ being short (e.g. 0.85cm for 20mT Cl2) compared to the chamber dimensions. The electrons and ions are predominately produced in the TCP's torroidal power deposition region, with the torroid pattern then being transferred to the wafer plane through ion diffusion. The trench depth pattern can be substantially reduced by operating at lower pressure <5mT, such that the λ_{mfp} is comparable to the chamber dimensions and energized electrons can ionize neutrals with almost equal efficiency across the chamber, where the shape of the plasma density determined only by ambipolar diffusion. However, this severely inhibits profile control with trench angle and selectivity requirements not being met.

This paper will discuss the work undertaken at Lam Research to characterize halogen plasma's produced by the TCP configuration of a Kiyo™ process chamber. Plasma diagnostic and simulation data shows that the plasma density uniformity can be substantially improved for a given pressure operation regime by optimizing the TCP hardware configuration. This optimization will translated into achieving <2.5% trench depth uniformity at mid pressure operation whilst maintaining profile control. Future challenges facing STI trench depth etch will also be discussed.

11:20am **PS1-TuM11 Control of TiN Sheet Resistance in Downstream Plasma PR Strip**, *V. Vaniapura,* ***L. Diao***, *S. Xu*, Mattson Technology, Inc.

Semiconductor integrated circuit density has increased continuously by shrinking the device size. Interconnects between multiple stacked metal layers need to be moved closer together hence thinner and narrower. However, the reduction of the interconnect dimensions increases electrical resistance and a subsequent loss of device performance. This leads to an ongoing effort to search for materials with lower electrical resistance suitable for interconnects to integrate into IC production. Metals like tungsten, titanium are good choices but require the use of conductive diffusion barriers. Titanium nitride (TiN) is widely employed as diffusion barrier layer and/or adhesion layer due to its low sheet resistance (Rs). Integration challenges occur with TiN during high temperature photoresist (PR) strip. The commonly used PR removal process, down stream oxygen plasma, can increase sheet resistance of TiN significantly. In order to understand how to reduce this adverse effect on the TiN layers, extensive studies of sheet resistance change (ΔRs) were conducted. TiN samples were treated with plasma exposure of different chemistries in an inductively coupled plasma reactor. Optical emission spectroscopy (OES) was used to observe the presence of reactive species in the plasma of different chemistries. The experimental results show that pure reducing chemistries were effective in maintaining the Rs, and the addition of these reducing chemistries to oxygen plasmas can significantly reduce ΔRs. OES analyses indicate that ΔRs is mainly caused by the oxidation of TiN with the present of reactive oxygen species in the plasma. Reactive oxygen content is controlled by the percentage of reducing chemistry in total flow. The dependences of ΔRs of TiN to various process parameters were investigated in detail. A majority of the Rs shift happens in the first tens of seconds of plasma exposure, which indicates that it is caused by modification of top surface. Based on this work, an optimized chemistry and process regime have been identified to greatly reduce or even suppress sheet resistance increase without compromising PR removal productivity.

11:40am **PS1-TuM12 Inductively Coupled Plasma Etching of GaN and Induced Defects**, ***J. Ladroue***, GREMI - STMicroelectronics, France, *A. Meritan, M. Boufnichel,* STMicroelectronics, France, *P. Lefaucheux, P. Ranson, R. Dussart*, GREMI, France

Wide bandgap materials such as gallium nitride are currently used for light emitter devices [1]. Otherwise, GaN physical properties open new prospects

in microelectronics manufacturing [2]. By combining a wide bandgap (3.4 eV), strong chemical bonds and high electronics mobility, GaN based devices should operate under higher temperature, higher power and higher frequency than typical silicon devices.

GaN etching is one of the first process steps in device structure developments. Due to inert chemical nature of GaN, wet etching is limited [3]. As a consequence, it is necessary to use dry etching method [4] to obtain a reliable MESA structures. Chlorine plasmas are commonly used because $GaCl_3$ is the most volatile etching product. Due to the strong bond energy of III nitrides, GaN etching also requires high physical sputtering which is provided by heavy neutral gas like argon and high bias voltage.

In this study, the GaN etching was performed into an industrial Alcatel 601 E tool which consists of an Inductively Coupled Plasma source and a diffusion chamber [5]. This high density plasma system was initially dedicated to silicon deep etching and modified to use chlorine gases. Plasma is generated by a single-ring antenna coupled to a RF power supply operating at 13.56 MHz. The 6 inch chuck is independently biased and thermally regulated. The process gases including argon and chlorine (Cl_2) are injected at the top of the source.

Cl_2/Ar plasma etching was performed on GaN epitaxial layers (12µm) grown on sapphire by metalorganic chemical vapor deposition (MOCVD). After SiO_2 deposition by Plasma Enhanced Chemical Vapor Deposition (PECVD), wafers were patterned using conventional photolithography. Samples were subsequently mounted on 6 inch coverplates made of different materials.

We have carried out a parameter screening to optimize the etch efficiency of GaN. The best results in term of profile quality are obtained with a silicon coverplate. An etch rate of 250 nm/min is reached with our current setup. However, defects like columns or pits are observed at the etched surface under some conditions. The origin of those defects is also investigated in this study. Moreover, diagnostics such as Langmuir probe, optical emission spectroscopy and mass spectrometry have been used to characterize the plasma and understand the etching mechanisms.

References:

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