Plasma Science and Technology
Room: A1 - Session PS+MS-MoA

Plasma Challenges at the 22nm Node and Beyond
Moderator: C. Labelle, GLOBALFOUNDRIES

2:00pm **PS+MS-MoA1 Plasma Etch Challenges for 22nm Advanced Logic Development**, ***R. Wise***, IBM **INVITED**

At the 22nm technology node for logic devices many novel semiconductor technologies are being considered, each of which impacts etch process development and control. These technology performance challenges drive increases in carrier mobility (necessitating application of high strain liner and epi materials and reduction in silicon loss budget and gate height scaling), increased packing density (limiting resist trim budgets, increasing CD shrink requirements, and increasing integration of eDRAM), and achieving target resistance and capacitance (necessitating the introduction of porous low-k dielectrics and better profile control). The challenges introduced by these elements on dry etch processes, tooling, and controls is discussed in detail.

Widespread aggressive device scaling beyond lithographic limits require dry etch processes to provide controllable CD reduction to meet design groundrules. In particular, limited improvement in imaging at the 22nm node results in challenges in scaling on the plasma equipment. The implementation of multiple exposure techniques to achieve design rules for several key levels drives additional process control across multiple exposure and etch steps. Reduction in the available mask thickness required to preserve the lithography process window have driven the need for highly selective etch processes, generally at the expense of uniformity, defectivity, and profile of the transferred pattern. Later generation lithographic materials are expected to continue to exhibit increased sensitivity to line edge roughness, and drive additional implementation of novel masking materials. Process and tooling technology needs required to address these imaging challenges are discussed.

2:40pm **PS+MS-MoA3 22nm Technology Manufacturing Challenges - Window for Process Control becomes Smaller and Smaller, Equipment and Material Interaction Becomes Unpredictable and Manufacturing Costs Increase**, ***P. Adam***, GLOBALFOUNDRIES Dresden, Germany **INVITED**

Increasing complexity and smaller and smaller CD for 22 nm technologies will have also a major impact for all plasma supported processes. The limited understanding of plasma and device interaction in existing technologies will further challenge the equipment suppliers to develop solutions for high volume manufacturing fabs. Some examples will be shown to illustrate this statement. Fab Engineers will see unexpected behaviour of materials in process chambers and surprising results of their plasma process on the device itself. A big amount of this will not be seen in the application labs of the equipment suppliers. Part of the problem is availability of appropriate test wafer material which can reflect the final manufacturing situation sufficient enough. Designs from different companies will behave most likely also differently. Therefore equipment suppliers have to move their development process close into the manufacturing site of the fabs. On the other side, semiconductor fab would like to get a tool and a process ready to go. They don't have the time and the manpower to support this kind of development work for the equipment supplier. All this will drive additional cost for both supplier and costumer.

How we can overcome this situation? Some ideas will be presented highlighting the complexity of the situation and the need for close interaction of all involved parties.

3:40pm **PS+MS-MoA6 Logic Etch Challenges at the 22nm Node and Beyond**, ***V. Vahedi***, *G. Kamarthy, J. Guha, H. Singh*, Lam Research Corporation **INVITED**

Due to increased device integration complexity, there are significant challenges to technology scaling for Logic devices at 22nm and beyond. The issues range from difficulties in scaling device threshold voltage (V_t), and electron and ion mobility enhancements to achieving the proper leakage current for low power devices. Proposed solutions to overcome these challenges include adoption of Metal Gate High-k for threshold voltage and leakage current engineering, to various Strained Silicon techniques to enhance electron and ion mobility, and FinFETs for beyond 22nm technology node. In this presentation, we will review some of challenges associated with front-end logic integration schemes, such as control of Si Recess and Si damage. Si loss and damage after gate etch, spacer etch, and strained Si etch applications can impact source-drain junction depth, and increase device leakage. We will discuss various mechanisms for Si loss and damage, work done by previous authors, what is required at 22nm and beyond, implication for etch and post etch clean, and areas where better understanding is required.

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