Tuesday Afternoon, November 10, 2009

Electronic Materials and Processing
Room: B1 - Session EM-TuA

High-K Dielectrics on High Mobility Substrates

Moderator: R.M. Wallace, University of Texas at Dallas

2:00pm **EM-TuA1 Process Evaluation for InGaAs n-Channel MOS Device**, *N. Goel,* Intel Assignee at SEMATECH, ***J. Huang***, SEMATECH, *H. Zhao,* University of Texas-Austin, *I. Ok,* SEMATECH, *J. Lee,* University of Texas-Austin, *P. Majhi,* Intel Assignee at SEMATECH, *P.D. Kirsch*, SEMATECH **INVITED**

With the fundamental limits to the aggressive device scaling in Si CMOS technology, there is significant ongoing research exploring alternate channel materials such as III-V and Ge. These materials hold promise to produce more power efficient transistors compared to current silicon technology. Due to their high carrier mobility, compound III-V semiconductors such as InGaAs and InSb, are being investigated in surface as well as buried channel devices where the inversion or majority carriers determine the device characteristics, respectively. The success of III-V in potential CMOS technology depend on heterogeneous integration on silicon with thinner buffer layers; compatible, low leakage and thermally stable gate dielectric with low interface state density; as well as defect free junctions with low external or access resistance. In addition it is key to develop, standardize and orient various physical and electrical characterization techniques to probe and evaluate the interface and bulk characteristics effectively and correctly at the atomic level. Significant amount of promising research is being done in these modules and there still remain several opportunities to reduce parasitic contributions.

2:40pm **EM-TuA3 Band Alignment at High-κ/III-V Interfaces Grown by Atomic Layer Deposition**, ***A. Wan***, *D. Mastrogiovanni, L. Yu, H.D. Lee, T. Feng, E. Garfunkel, T. Gustafsson,* Rutgers University, *M. Xu, P. Ye*, Purdue University

Band offsets and Fermi level pinning are extremely important issues for metal-oxide-semiconductor (MOS) device structures. In particular, there is increased interest in III-V semiconductor/ high-κ dielectric materials as a future replacement to conventional Si-based complementary MOS technology. In this work, we present band alignment measurements of Al2O3 grown by atomic layer deposition (ALD) on n-GaAs and p-GaAs by combined x-ray (XPS) and ultraviolet (UPS) photoemission spectroscopy. Influence of processing conditions (pre-growth, during growth, and post-growth) and substrate orientation on the Fermi level pinning is discussed. Pinning effects are more problematic on n-GaAs than p-GaAs, due in part to the fact that n-GaAs more readily forms As oxides that have been attributed to high interface gap state densities that cause pinning. Interestingly, at the first few layers of ALD grown at "self cleaning" conditions,[1, 2] native oxides on the GaAs for both n-type and p-type are significantly reduced, but the interfaces on n-GaAs are still strongly pinned. Best results for un-pinning of the Fermi levels between n-GaAs and p-GaAs is observed for Al2O3 / GaAs(111) samples having clean interfaces, grown at condition, and post-deposition annealing at 600° C in forming gas.

1. M. M. Frank, G.D.W., D. Starodub, T. Gustafsson, E. Garfunkel, Y. J. Chabal, J. Grazul, and D. A. Muller, Appl. Phys. Lett. 86, 152904 (2005).

2. H.D. Lee, T.F., L. Yu, D. Mastrogiovanni, A. Wan, T. Gustafsson, and E. Garfunkel, Appl. Phys. Letters (submitted), 2009.

3:00pm **EM-TuA4 Reduction of Native Oxides on GaAs during Atomic Layer Deposition of Al_2O_3**, ***H.D. Lee***, *T. Feng, L. Yu, D. Mastrogiovanni, A. Wan, T. Gustafsson, E. Garfunkel*, Rutgers University

The integration of high-*k* dielectrics with high mobility III-V semiconductors is important due to the need for higher speed and lower power electronic devices than are offered by Si-based technologies. While high-*k* dielectric deposition on GaAs and InGaAs semiconductors appears particularly promising, the removal of native oxides and the growth an ideal dielectric layer remains a serious challenge. This obstacle arises in part from the high density of defects present at most GaAs-dielectric interfaces, and is related to Fermi-level pinning at the interface. Several groups have shown that chemical cleaning and subsequent passivation of the interface prior to dielectric deposition can greatly reduce the interface state density (D_{it}). However, few passivation solutions are practical for future large scale CMOS device manufacturing.

Although several studies (including our own) have shown the reduction of native oxides on GaAs and InGaAs during atomic layer deposition (ALD) of dielectrics, detailed structural and chemical information about the interface and reduction process have not been reported. We have examined depth profiles of the elements in native oxides and ALD-deposited Al_2O_3 layers on GaAs substrates with an integrated tool that enables ALD growth with *in situ* characterization by medium energy ion scattering spectroscopy (MEIS). Films were also analyzed by x-ray photoelectron spectroscopy (XPS).

We will present data on the reduction of surface "native" oxides from GaAs substrates following reactions with trimethylaluminum (TMA) precursor. MEIS and XPS measurements after one single TMA pulse without oxygen exposure show that ~65% of the native oxide including ~75% of the As oxides are reduced, and a 5Å oxygen rich aluminum oxide layer is formed. XPS also shows that 3 additional TMA pulses reduce all As oxides to a level below our detection limit, and the Ga oxides were also reduced substantially. Further MEIS study of Al_2O_3 grown with the normal atomic layer deposition cycles of TMA and water shows that the growth rate of Al oxide during the reduction of native oxides is faster than the rate after the reduction. The preferential interface reduction of native oxides (especially AsO) helps create a higher capacitance, lower interface defect density CMOS gate stack.

4:00pm **EM-TuA7 Arsenic-dominated Chemistry in the Acid Cleaning of InGaAs and InAlAs Surfaces**, ***Y. Sun***, Stanford Synchrotron Radiation Lightsource, *P. Chen, M. Kobayashi, Y. Nishi,* Stanford University, *N. Goel, M. Garner, W. Tsai,* Intel Corp., *P. Pianetta*, Stanford Synchrotron Radiation Lightsource

The surface cleaning of InGaAs and InAlAs is studied using Synchrotron Radiation Photoelectron Spectroscopy. Thermal annealing at 400ºC can not completely remove the native oxides from those surfaces. Elemental arsenic build-up is observed on both surfaces after acid treatment using HCl, HF or H_2SO_4 solutions, which is similar to acid-cleaned GaAs surface. Cleaned InGaAs surface is oxide free but small amount of aluminum oxide remains on cleaned InAlAs surface. The common chemical reactions between III-As semiconductors and acid solutions are identified and are found to be dominated by arsenic chemistry.

4:20pm **EM-TuA8 Wet Treatment for Se Surface Passivation of GaAs and Ge for Advanced CMOS Applications**, ***F.S. Aguirre-Tostado***, CIMAV-Monterrey, México, *A. Herrera-Gómez,* CINVESTAV-Qro, México, *R.M. Wallace*, University of Texas at Dallas

Surface passivation of III-V and Ge semiconductors is a remaining problem to realize CMOS scaling beyond the 22 nm technology node. Zinc-blende and diamond structure (100) surfaces could be passivated with a single monolayer of divalent atoms like S or Se. In this presentation we show a wet chemical treatment method for the passivation of III-V and Ge (100) substrates with Se and S. The treatment consisted of the dipping of the substrates on a dilution of metallic Se into a 22% ammonium sulfide solution. The treated surface showed 3D structures that are attributed to either clustering during the treatment or during the N2 drying step. AFM, SEM and XPS were used to analyze the surface morphology of the passivation layer and chemical bonding with the substrate atoms. C-V and J-V characteristics of MOS capacitors with and without Se passivation are discussed.

4:40pm **EM-TuA9 The Effect of "Self-Cleaning" ALD Growth on the Electrical Properties of Metal/ High- κ /GaAs and Metal/high-κ/Ge Metal/ MOS Capacitors**, ***L. Yu***, *H.D. Lee, T. Feng, D. Mastrogiovanni, A. Wan, T. Gustafsson, E. Garfunkel*, Rutgers University

The ideas of using high-κ dielectrics as gate oxide and high mobility semiconductor as channel material are promising means of prolonging the scaling of CMOS technology to post Silicon era. However, it has been extremely challenging to produce a high quality oxide/channel interface that yields sufficient device performance for future CMOS. The unwanted chemical species such as residue native oxide, surface carbon, and hydro-carbon can result in defect states at the interface or inside dielectrics. These states can enhance carrier scattering and degrade device threshold voltage. Several recent studies, including ours, showed that, above certain temperature, volatile metal-organic precursors such as TMA can chemically react with the native oxides on the GaAs or InGaAs surface, result in effective removal of native oxide species, and chemically clean interface. This effective is known as the "self-cleaning" ALD growth. Previous studies are largely based on *in situ* XPS and MEIS measurements on ALD grown samples at various stages during the first few cycles. In this work, we will report on the effect of "self-cleaning" ALD growth and post ALD forming gas annealing on the electrical properties of metal/Al_2O_3/GaAs

MOS capacitors. We found the combination of the two treatments can significantly enhance the device C-V characteristics. Our preliminary results showed that frequency dispersion of ~2% per decade in the accumulation capacitance and interface state density (D_{it}) of ~$5x10^{12}$ eV^{-1} can be achieved. We also correlated the electrical result with XPS and MEIS studies of the ALD grown Al_2O_3 films and as well as electronic structure at Al_2O_3/GaAs interface. We will also report on the "self-cleaning" growth study of high-κ (Al_2O_3 and HfO_2) on Ge substrate and corresponding electrical result on MOS-CAPs.

5:00pm **EM-TuA10 Characterization of the "Clean-Up" of the Germanium Surface by ALD using Trimethyl Aluminum and Water**, ***M. Milojevic***, University of Texas at Dallas, *R. Contreras-Guerrero, M. Lopez-Lopez,* CINVESTAV-IPN, Mexico, *J. Kim, R.M. Wallace*, University of Texas at Dallas

The "clean-up" effect on III-V substrates has recently been well documented.[1] For the purpose of this study the "clean-up" of Ge oxides by ALD is explored using XPS. By interrupting the ALD process following individual precursor pulses for in-situ monochromatic XPS analysis the reaction mechanisms can be studied in unprecedented detail. As in the case of III-V substrates native germanium oxides are found to be reduced strongly by TMA. Interestingly if the sample is treated with a plasma nitridation technique a GeON layer is grown that appears impervious to this reaction. This is not unexpected given the reports of the stability of GeON formed by ion rather than radical based plasma processes.[2] Oxide free germanium surfaces behave analogously to a surface with initial native oxides since they are oxidized measurably prior to the first TMA pulse due to residual oxidants in a commercial ALD chamber. The unique aspect of the TMA driven "clean-up" is exposed when comparing it to the reduction of interfacial oxides by a thin metallic aluminum layer.[3,4,5,6] In this case in addition to the reduction of germanium oxides the aluminum layer also results in Ge-Al bond formation. In contrast "clean-up" of the oxide by TMA is characterized by a preferential reduction of higher oxidation states of germanium and the absence of any detectable reduction products on the surface.

This work was supported by the FCRP Focus Center on Materials, Structures and Devices and the Texas Enterprise Fund.

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[6] Margaritondo et al., J. Vac. Sci. Technol. A 1(2), Apr/Jun 1983

5:20pm **EM-TuA11 Processing Controlled Substrate Reactions for Deposition of Monoclinic Textured HfO_2 Thin Films on Pre-Oxidized and Nitrided Ge (001) Substrates**, *K.B. Chung, L. Miotti,* ***K.P. Bastos***, North Carolina State University, *D. Nordlund,* Stanford Synchrotron Research Lightsource (SSRL), *G. Lucovsky*, North Carolina State University

2 nm thick films of HfO_2 have been deposited on Ge(001) substrates by remote plasma chemical vapor deposition for (i) multiple etching cycles in dilute HF followed by distilled water rinsing, and (ii) an in situ remote plasma-assisted nitridation (RPAN) process. In a second set of studies, the step(i) pre-clean was replaced by a basic re-clean using methanol and NH_4OH. Studies by X-ray absorption spectroscopy (XAS) in O and N K edge regimes, were used to monitor HfO_2 nano-grains morphologies. Previous studies indicated epitaxial textured HfO_2 and TiO_2 films were obtained on Ge(001) surfaces. However, these studies were based on a recipe that worked, and did provide insights to significant connections between pre-cleaning and post deposition annealing. We have found two aspects of processing are crucial, and these were evaluated spectroscopically. Electrically active defects in metal-oxide-semiconductor test devices indicated high-defect densities correlated directly with Ge and O reacting with HfO_2 in the interfacial transition region, resulting in mixed-morphology grains.

Interfacial and bulk film degradation are also detected in XAS O K edge measurements. The occurrence of a monoclinic (m-)HfO_2 E_g edge structure is associated with Ge-O free interfacial transition regions. Ge-O interfaces results in tetragonal (t-)HfO_2, or mixtures of t-HfO_2 and m-HfO_2 grains. Acidic and basic pre-cleans each followed by an RPAN process prevented reactions between Ge-O surface bonding and plasma-excited HfO_2 precursors, consistent with textured m-HfO_2 films. Spectroscopic ellipsometry indicated that Ge-O bonding was significantly higher for acidic pre-cleans compared with basic pre-cleans. Post deposition annealing cycles with textured m-HfO_2 films were consistent with this difference. Two step annealing after the acidic clean, the first at 550°C in Ar, and the second at 800°C in Ar, resulted in textured m-HfO_2 directly in contact with a reconstructed Ge(001) surface. N K edge XAS, had previously indicated complete release of N after annealing to 700°C in Ar. In contrast, with less Ge-O interfacial bonding in the basic pre-clean, Ge-O and Ge-N interfacial bonds were eliminated sequentially during an 800°C anneal in Ar. O K edge XAS for HfO_2 with the X-ray polarization in the direction of the dimer rows of Ge(001) wafers, or perpendicular to that direction indicated similar textured growth. This is consistent with the textured m-HfO_2 films having nano-grains aligned at ±45° relative the dimer row direction.

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