Plasma Science and Technology
Room: 306 - Session PS2-FrM

Plasma Processing for 3-D Integration, Photonics, Optoelectronics, and Memory Devices
Moderator: C.C. Hsu, National Taiwan University

8:20am **PS2-FrM1 Silicon Oxide Sidewall Passivation during HBr Inductively Coupled Plasma (ICP) Etching of InP and GaAs Materials for the Fabrication of Photonic Devices**, ***S. Bouchoule**, S. Guilet, L. Gatilova, G. Patriarche, L. Largeau,* LPN, CNRS, France, *P. Chabert*, LPTP, CNRS - Ecole Polytechnique, France

The ICP etching technique is now widely used for the anisotropic etching of III-V heterostructures, a key building-block for photonic devices. Chlorinated atmospheres are generally used for both InP and GaAs materials, with few studies devoted to HBr. In any case, very few studies exist on the understanding of the sidewall passivation mechanisms occurring during the etching of III-Vs. Using EDX-TEM ex-situ analysis, we have shown for the Cl2-H2 chemistry [JVSTB 26, 666 (2008)] that a silicon oxide layer acting as a lateral etch-inhibitor can build-up on the etched sidewalls of InP-based heterostructures, when a Si wafer is used as the sample tray. This configuration corresponds to most commercial ICP etch systems having an electrode diameter of 4-in or more, used to etch III-V samples of 2-in or less size. In this work, we have analyzed by ex-situ EDX-TEM the passivation layer deposited on the sidewalls of InP and GaAs pillars etched with HBr using a Si tray. A Si-rich layer can build-up on the etched sidewalls under low pressure and high ICP power conditions, leading to anisotropic profiles. The passivation mechanism resembles that identified in Si gate etching using Cl2-HBr-O2 plasmas, and we suggest that a minimum amount of oxygen should exist in the plasma for the passivation layer to build-up. OES measurements indeed showed that oxygen is present in the gas phase, even w/o intentional O2 addition. In our conditions (0.5 mT–1 mT pressure range and ~1000 W ICP power), high values of plasma potential (> 20V) and positive ion current (> 3 mA/cm2) are measured, and oxygen could come from the sputtering of either the Al2O3 ceramic inner parts or the passivated walls of the reactor. We identified that the walls state greatly influences the sidewall passivation process, indicating that the species desorbed from the conditioned walls play an important role. Moreover, we show that adding less than 10 % of O2 to the gas mixture can modify the passivation mechanism: it is strongly enhanced in the case of GaAs material, and the layer is changed from a Si-rich layer to a more stoechiometric SiO2 in any case. The InP and GaAs planar etch rate is also increased, to the benefit of selectivity against dielectric mask, indicating that the concentration of reactive radicals is modified by the addition of a small amount of O2 in HBr. Low loss laser ridge waveguides on InP(311)B substrate and AlGaAs/GaAs microcavities are demonstrated with the optimized process.

8:40am **PS2-FrM2 Low Bias Inductively Coupled Plasma Etching of CdHgTe in CH_4/H_2 Based Chemistry**, ***F. Boulard**, C. Cardinaud,* IMN CNRS France, *J. Baylet*, LETI-CEA, MINATEC France

CH_4/H_2 based dry etch chemistry is still under study for patterning of high aspect ratio trenches or holes in II-VI compound semiconductor cadmium mercury telluride ($Cd_xHg_{1-x}Te$) used for high performance infrared detectors.[1] Since energetic ions bombardment induces electrical damages,[2] development of a gentle, low bias and chemistry assisted process is investigated. Plasma diagnostics and materials characterizations are developed to obtain a better description of etching fundamental mechanism. Inductively Coupled Plasma (ICP) reactor, allowing decoupling of plasma generation and substrate polarization, is used. Process parameters under study include gas mixture (using CH_4, H_2, N_2 and Ar), bias voltage, source power and substrate holder temperature. Experiments are carried out on alloys which composition varies from x=0.23 to 1. Langmuir probe and mass spectrometry measurements are used to correlate plasma modification induced by N_2 addition to the gas mixture with etched surface characteristics and etch rate. Etch product identification confirms the formation of TeH_2, while direct evidence of $Cd(CH_3)_2$, as proposed in the literature[3,4] is discussed. Post etch quasi in-situ X-ray photoelectron spectroscopy and spectroscopic ellipsometry suggest that etching occurs through a carbonaceous, Cd-rich and Hg-depleted layer. When the bias is significantly decreased to a value as low as 10V and the substrate holder temperature is raised, an average etch rate increase and a strong reduction of the extreme surface Cd/Hg ratio are observed, confirming an enhancement of chemically assisted elimination of Cd. The process developed offers smooth, mirror like, surface morphology and etch rate higher than 300nm.mn^{-1} on $Cd_{0.23}Hg_{0.77}Te$.

[1]A. Rogalski, Infrared Physics and Technology, 50 (2007) 240-52
[2]E. Elkind, J. Vac. Sci. Technol., A 10 (4), (1992), 1106-12
[3]R.C. Keller, M. Seelman-Eggebert, H.J. Richter; J. of Elec. Mat, 24 (9), (1995), 1155-1160
[4]C.R. Eddy, D. Leonhardt, V.A. Shamamian, J.R. Meyer, C.A. Hoffman, and J.E Butler, J. Elec. Mat., 28 (4), (1999), 347-54.

9:00am **PS2-FrM3 Characterisation of InP Ridge Sidewalls Patterned in Inductively Coupled Halogen Plasmas**, ***C. Cardinaud***, IMN-CNRS, France, *S. Bouchoule*, LPN-CNRS, France

High-aspect-ratio etching of InP-based heterostructures is a critical building block for photonic device fabrication. Indeed highly anisotropic profiles and smooth sidewalls free from undercuts or notches are required to minimize optical scattering losses. Recently it was shown that anisotropic etching can be obtained in Cl2-H2 and HBr inductively coupled plasmas (ICP), due to the passivation of the InP sidewalls by a Si-containing layer originating from the Si sample tray [JVSTB 26(2008)666]. This study is focused on the chemical characterisation by means of X-ray photoelectron spectroscopy of the bottom and sidewall surfaces of InP ridge patterns etched with Cl2-H2 and HBr chemistries. Anisotropic profiles are obtained for low pressure (<1mT), high ICP power (up to 1000W for HBr), H2 percentage (H2%) in the 35-45% range for the Cl2-H2 mixture, moderate dc bias (-140V), sample temperature of ~190°C. ICP etching results are compared to HCl wet etching, taken as reference. Surface chemistry at the pattern bottom can be summarized as follows. Etching in Cl2-H2 with a H2% ~36% gives a surface very close to HCl. Width of the P2p, In3d and In4d InP-bulk contributions are very close to the reference, this indicates that no other species than the oxide is present above the bulk material. The intensity ratios for In/P-bulk (0.9) In/P-oxide (0.6) point out that Cl2-H2 etching produces a slightly P-rich surface. In the case of HBr, the much larger width of the InP-bulk components suggests the occurrence of an additional species that could be amorphous InP. Moreover, an extra component is observed on the P2p spectrum at +0.8eV from that of InP-bulk. In the absence of Br from the surface, we suggest attribution to P-H species. Finally, the high In/P-bulk and In/P-oxide ratios, 4.3 and 3.9 respectively, clearly state that HBr produces an In-rich surface. Sidewall chemistry shows significant differences as compared to the bottom. For example in the case of Cl2-H2, the P2p, In3d and In4d InP-bulk contributions are about 1.5 times larger. Moreover the In/P ratio falls down to 0.4 and about 0.1 for In/P-bulk and In/P-oxide respectively. Opposite, the HCl etched sidewall is identical to the bottom (In/P-bulk = 0.9). For Cl2-H2 etching, this definitely points out a variation of composition in the top 10nm, with a decreasing In/P ratio from the “bulk” to the sidewall surface. Similar analysis are presently carried out on HBr and HBr-O2 etched samples.

9:20am **PS2-FrM4 The Plasma Polymerization of Novel Metal Containing Monomers Via Sublimation of the Precursor Materials**, ***J.O. Enlow**,* UES, Inc., *H. Jiang,* Materials Sci. and Tech Applications, LLC, *J.T. Grant,* University of Dayton, *K.G. Eyink,* Air Force Research Laboratory, *W. Su,* AT&T Government Solutions, *A.M. Urbas, T.J. Bunning*, Air Force Research Laboratory

A flowing afterglow plasma reactor has been recently modified to incorporate a custom designed sublimation system for the fabrication of thin films from solid organic monomers. Some metal containing precursors such as ferrocene, as well as Cu, Fe, Mg, Ni, Pb and Zn phthalocyanines and porphorines have been successfully deposited. The optical properties of the films were investigated using variable angle spectroscopic ellipsometry and UV-Vis spectrometry, the chemical composition was determined using FT-IR and XPS and the morphology was examined using AFM and X-ray reflectivity. It was found that due to the incorporation of metal components, these films have relatively high indices of refraction when compared to conventional PECVD hydro-carbon films. Also, through the optimization of the deposition conditions original structural features were maintained in these highly crosslinked thin films. This study demonstrates that the use of sublimation opens up the PECVD technique to a wealth of new solid state and metal containing materials for the fabrication of novel optical and electronic thin films.

9:40am **PS2-FrM5 Advancement and Characterization of 3D TSV Etch Applications**, ***C. Rusu***, Lam Research **INVITED**

Implementation of TSV modules in production for 3DIC applications has become a technical and fundamental reality to contend with. Almost every semiconductor manufacturer is either directly working on TSV module design and development, or – if fabless, is working with partners for implementation of TSV modules. It is clear that CMOS Image Sensors (CIS) are leading the pack in implementation, with memory suppliers

following closely. However, it is unclear at this time which memory segment will choose to implement TSV's first; DRAM or Flash, perhaps for reasons more related to economics than technology. This talk will primarily focus on the etch requirements for the TSV module. Etch challenges can vary widely with different applications, such as CIS, Memory, or Logic. In addition, TSV etch challenges vary for different integration schemes, such as via first, via middle, or via last. Therefore, it is without surprise that the TSV etch development tasks have been quite challenging, and existing etch equipment were not immediately applicable for TSV implementation. Recent development and upgrades have been made to address these market requirements, whether for silicon or glass substrates. We will show results of a flexible process system that can etch the multi-film stacks in addition to the deep silicon required to form TSVs. Substrates are patterned with either photoresist or dielectric hard mask, ranging from the micron-level minimum geometries to several tens of microns. TSV etch examples will be demonstrated addressing different integration requirements ranging from patterned photoresist directly on silicon, to patterned photoresist on multi-stack films replicating some of the layers that may exist on processed IC wafers.

10:20am **PS2-FrM7 Investigation of Bottom Profile Degradation Mechanism in Extremely High-Aspect-Ratio Feature Etching**, ***N. Negishi***, *M. Miyake, K. Yokogawa,* Hitachi, Ltd., Japan*, M. Oyama, T. Kanekiyo,* Hitachi High-Technologies Corporation, Japan*, M. Izawa*, Hitachi, Ltd., Japan

As the half-pitch of DRAM design rule advances beyond the 50 nm, precistion plasma etching will be required to realize extremely high aspect ratio feature of over 30. According to the shrinkage of pattern CD and narrowing pattern pitch size, many kinds of profile degradations that occur especially at around bottom area, such as, bottom distortion, twisting, shortage of bottom CD, have been observed. We assume that the mechanism of these etching profile degradations has closely connection with the combination of mask profile deformation, charge-up phenomenon, and the change of etch-front condition at bottom region. In order to diminish these profile degradations, we investigated the mechanism in terms of mask profile deformation effect with using ultra-high-frequency ECR (UHF-ECR) plasma etching system.[1] In this study, we used trench pattern to evaluate the degree of pattern deformation quantitatively as a function of pattern depth. Also, direct observation of etched pattern sidewall with using atomic-force-microscopy (AFM) was applied to clarify the relationship between bottom distortion and mask (necking) profile. The ratio of line width roughness (LWR) to line edge roughness (LER) that estimated from top view observation of etched sample after etch-back process decreased with increasing pattern depth and it means that pattern deformation becomes to 'wiggling' mode at deeper area. On the other hand, AFM observation of etched sidewall revealed that mask (necking) roughness is transferred to the bottom region and amplified drastically. As a result, we confirmed that using the mask of low degree of deformation is effective to diminish the bottom distortion.

(1) K. Yokogawa, N. Negishi, S. Yamamoto, K. Suzuki, and S. Tachi, 1997 Dry Process Symp., pp. 379-383.

10:40am **PS2-FrM8 Very Uniform and High Rate Si Etching Process in Advanced NLD Plasma**, ***Y. Morikawa***, *T. Murayama, K. Suu*, ULVAC, Inc., Japan

High-density of thru silicon via (TSV) is indispensable to the utilization and improvement in performance in 3D-LSI. Advanced high aspect ratio (A/R) TSV etching technologies are required for high-density TSV formation. We have developed a new etching system for TSV and MEMS application. This System provides combined plasma of magnetic neutral loop discharge (NLD) plasma and a sputtering system, which is named as NLD-Si.[1] For high rate silicone etching, it is very important to understand not only high density of the plasma generation but relation between fluorine diffusion (Z: distance of a wafer stage and NLD plasma) and the etching characteristic. In this study, a novel RF antenna 'multi slit rf antenna' has developed for the purpose of high rate etching. The number of slits of the antenna was increased from single line to three parallel lines to extend inductive coupling discharge region. Therefore, high-density generation of both of ion radicals is possible. Each slit interval is 25 cm. And, it is the feature that inductance (L) of this antenna is 0.52 uH and it is low L antenna. As a result of performing electron density measurement of the NLD plasma using this MS-RF Antenna, it succeeded in the high-density plasma production of $1x10^{12}$ / cm^3 by the process pressure of 2 Pa. Next, Si etching process development was performed using the Advanced NLD-Si etcher, which introduced a wafer stage elevator system. Si etching characteristics employing advanced NLD plasma were studied with respect to distance from an antenna. As a result, improvement in the etching rate of 2.5 times or more was realized as a result of optimization of the distance from NL. And, when process pressure and flow rate conditions were made to optimize, about 5 times the etch rate UP was achieved. Finally, the pattern of line width 1um attained the anisotropic etching of 8.5 um/min using Advanced NLD-Si etcher.

[1] Y. Morikawa, et al.; Thin Solid Films 515 (2007) 4918.

11:00am **PS2-FrM9 Fabrication of Very High Aspect Ratio Vertical Through Silicon Via by a Novel Multi-step Plasma Etching Technique**, ***P. Dixit***, Nanyang Technological University, Singapore*, R. Chatterjee,* Georgia Institute of Technology*, J. Miao,* Nanyang Technological University, Singapore*, R. Tummala*, Georgia Institute of Technology

In this paper, we present a novel multi-step etching technique to encounter the aspect ratio dependent etching (ARDE) characteristic of plasma etching process and to fabricate very high aspect ratio vertical through silicon vias. ARDE effect, which represents the reduction in etch rate at higher etching depth, is caused by the the depletion of etching radicals. The collisions of etching species with the outgoing reactions products and with the sidewalls, are also responsible for reduction in the etch rate. To maintain the constant etch rate and vertical sidewall profile, the depletion in the etching radicals should be compensated, which can be achieved by adding more etching radicals and plasma energy. To achieve this objective, we have proposed a multi-step etching technique, in which important DRIE parameters were gradually increased to maintain the constant etching flux . DRIE parameters, such as platen/coil power, SF6 and C4F8 flow rate, etching and passivation cycle duration, etc were increased in steps to provide 'additional etching species' needed at the bottom of the high aspect ratio etched features. At first, effect of individual parameters was investigated by varying a single parameter while keeping remaining parameters constant. 6 DRIE experiments were carried out to evaluate the effect of platen power on the etched profile (8, 10, 12, 14, 16 and 18 W). Similarly other experiments were performed to find the best parameter to overcome the depletion of etching radicals and to maintain the vertical etch profile. When the effect of individual parameters on etched profile was known, those parameters were chosen that gives the straight profile at relatively higher etch rate and with minimum undercut. Effect of platen power on controlling the perpendicularity of through-vias was found to be the most dominant among all parameters. A 200 nm aluminum layer was used as an anti-notching layer to prevent the lateral etching of vias at the bonding interface. Scanning electron microscope confirmed that the etching profile was completely vertical even at an etching depth as large as 510 micron. Using this technique, very high aspect ratio (>30), vertical through silicon vias having an opening dimension as small as 10 micron were fabricated. These DRIE etched through silicon vias were later electroplated to form copper interconnects, which are the most important building blocks for the next generation 3D stacking technology.

11:20am **PS2-FrM10 Through Silicon Via Etching for 3-D Interconnection using Pulse Inductively Coupled Plasma**, ***S.H. Lee***, *Y.D. Lim, W.J. Yoo,* Sungkyunkwan University, Korea*, O. Jung, S.C. Kim, H.C. Lee*, Dongbuhitek, Korea

Deep Silicon via etching technology is considered to be a critical and important factor to connect three-dimensional (3D) integrated-circuit system. In this process, the formation of deep Si via etching profiles is an important factor to accomplish filling of the highly conductive metal-materials and operating device in package level. We studied a non-Bosch type deep etching method using the pulse inductively coupled plasma (ICP) for the purpose of improving high aspect-ratio etching profile and reducing undercut at the entrance of the Si vias. We used an ICP etcher (ICP) in which wafer electrode is equipped with pulsing RF bias power which enabled the control of frequency, duty cycle and thereby was expected to affect ion acceleration onto the wafer surface and sidewall passivation of SiOxFy. SF6, O2, and Ar were used to accomplish deep non-Bosch –type Si etching for the pulse plasma discharge. To understand the effects of radicals in the plasma on the formation of etching profiles of deep Si vias, we monitored optical emission of radicals at 419.6 nm for Ar, 703.6 nm for F, and 777.0nm for O.

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