Tuesday Morning, October 21, 2008

Plasma Science and Technology
Room: 304 - Session PS-TuM

Advanced Gate Etching
Moderator: Y. Zhang, IBM

8:00am **PS-TuM1 High Density Plasma Etching of Titanium Nitride Metal Gate Electrodes for FDSOI Sub-Threshold Transistor Integration**, ***S.A. Vitale***, *J. Kedzierski, N. Checka, C.L. Keast*, MIT Lincoln Laboratory

Dual work function band-edge metal gate electrode materials are replacing polysilicon gates at the 45nm technology node for high performance CMOS logic production. At the same time, mid-gap metal gate electrodes are being considered to replace polysilicon gates in novel fully depleted silicon-on-insulator (FDSOI) ultra-low power CMOS devices. A discussion of the physical and electrical requirements of the gate materials for these two technologies will be presented, along with an introduction to the "gate first" vs. "gate last" integration approaches. Titanium nitride metal-gated capacitors and transistors have been successfully fabricated, on a conventional SiO2 gate dielectric. C-V curves have been measured and fit to a quantum-corrected model, with a measured workfunction of 4.55eV. Gate oxide breakdown data reveals a charge-to-breakdown approximately 10x lower than that of conventional polysilicon/SiO2 gates, and a discussion of how this may be improved using a HfO2 high-k gate dielectric will be presented. A key challenge of integrating metal gates is the plasma etching of the gate stack. Conventional etching of a polysilicon layer above the TiN results in a large foot at the base of the polysilicon, due to the presence of the conducting TiN film. TiN etch selectivity over SiO2 in excess of 40:1 is achieved by measuring and exploiting the difference in ion enhanced etching threshold energy between these films. TiN is shown to etch spontaneously in HBr plasmas due to the thermodynamically favorable Ti + Br reaction, but is strongly inhibited in the presence of oxygen. TiN etching in high density plasmas exhibits a strong aspect ratio dependent etching (ARDE) effect, which can be minimized by using a two-step etch process, with different neutral-to-ion flux ratios. *This work was sponsored by the Air Force under contract #FA8721-05-C-0002. Opinions, interpretations, conclusions, and recommendations are those of the author and are not necessarily endorsed by the United States Government.

8:20am **PS-TuM2 TaN Etch Mechanisms in BCl_3-based Plasmas**, ***D. Shamiryan***, IMEC, Belgium, *A. Danila*, Moscow Institute of Electronic Technology, Russia, *V. Paraschiv, M.R. Baklanov, W. Boullart*, IMEC, Belgium

TaN is a potential candidate for metal gates. BCl_3 plasma is used to pattern metal gates as it has high selectivity over Si substrate and etches metal oxides (native oxides on metal gates and high-k dielectrics). During metal gate etch in inductively coupled plasma reactor, we found that TaN gate profile depends on the composition of BCl_3-based plasma. Pure BCl_3 results in an undercut of TaN. The undercut can be avoided by addition of 5% O_2, further increase of O_2 concentration (till 10%) does not change the TaN profile. When N_2 is added to BCl_3 plasma, first the undercut disappears (at about 6% of N_2) and then a slope appears as N_2 concentration increases further (toward 10%). To clarify the etch mechanisms, we studied etching of blanket TaN wafers (30 nm film deposited by PVD). To avoid ion bombardment and simulate conditions on the sidewalls of a gate, the substrate bias was set to zero. Etch rate of TaN was measured by spectroscopic ellipsometry; surface composition was examined by XPS. In the case of pure BCl_3 plasma a thick film (deposition rate of 20 nm/min) is formed. The film consists of B (50%), Cl (30%) and O (20%). The oxygen probably comes from the oxidation on air between the etching and the XPS measurements. When 5% of O_2 is added, no film is observed, the surface composition is close to as-deposited TaN (with some B added). We observed strong peaks in emission spectra of BCl_3/O_2 plasma, attributed to BO_x. When 5% N_2 is added to the BCl_3 plasma, a film of the same thickness as for pure BCl_3 is observed, but it contains less Cl (15%). We propose the following etch mechanism. In pure BCl_3 plasma a Cl-containing film is deposited on the sidewalls of the gate. Cl from the film reacts with TaN producing an undercut. When O_2 is added, no film is formed and the TaN profile is straight as B apparently reacts with O in the gas phase, forming volatile BO_x radicals. Further increase of O_2 content does not change the profile as no film is formed (until O_2 concentration reaches 50% when B_2O_3 film is deposited). When N_2 is added to BCl_3, a film is formed but in this case N_2 replaces Cl and the film becomes passivating leading to a straight TaN profile. As more N_2 added, the film passivates TaN more efficiently leading to a sloped profile.

8:40am **PS-TuM3 Etching Profile Simulation of Metal/High-k Dielectric HfO_2 in Chlorine Based Chemistry**, ***T. Yagisawa***, *T. Makabe*, Keio University, Japan

With continuous downscaling of complementary CMOS devices, the physical thickness of SiO_2 gate dielectric is requested to be reduced to sub-micrometer regime. When the thickness is less than 1 nm, gate dielectric cannot satisfy the requirement of the low standby power CMOS devices beyond 32 nm technology node in 2013, due to the increase of gate leakage current, poly-Si gate depletion, and dopant penetration into the channel region. In order to overcome these issues, extensive studies to replace conventional poly-Si/SiO_2 with metal/high-k gate stack have been carried out. Among several candidates, HfO_2 attracts considerable attention because of its thermal stability at the interface with Si. It is well known, chlorine based chemistry is more suitable for the plasma etching of high-k dielectric HfO_2 than fluorine chemistry due to the high volatility of the etched by-products. One of the most promising procedures to etch metal/HfO_2 gate stack is Cl_2/O_2 plasma where high selectivity can be obtained over underlying Si and SiO_2. In addition, the etching residues made of Hf chloride may not be volatile in a low temperature condition. This leads to a significant adsorption at the sidewall, resulting in a variation of surface roughness (LWR: line width roughness). Thus, the etching profile of high-k material has strong dependence on substrate temperature. In this paper, the etching profile of high-k HfO_2 film is numerically predicted in the chlorine based chemistry in a two-frequency capacitively coupled plasma. Dependence of LWR on the substrate temperature will be mainly discussed by considering the redeposition of etched by-products ($HfCl_xO_y$) inside the pattern. Emphasis will also be given on the selectivity of HfO_2 etching over Si and SiO_2.

9:00am **PS-TuM4 Reaction Mechanisms in Patterning Hafnium-Based High-k Thin Films**, ***R.M. Martin***, *J.P. Chang*, University of California, Los Angeles

As hafnium-based oxides are being implemented into sub-45nm CMOS devices, the corresponding development of an enabling plasma etching chemistry is necessary for patterning these new gate dielectric materials. In this work, an electron cyclotron resonance high density plasma reactor was used to study the etching of hafnium aluminates and nitrided hafnium silicates with varying compositions in chlorine-based chemistries. In general, the measured etch rate for these materials scaled with the square root of ion energy at high ion energies (> 50 eV), however the etch rates in BCl_3 was 4 to 7 times that in Cl_2, due to the change in the dominant ion from Cl_2^+ to BCl_2^+. The composite oxides were found to etch faster than the simple oxides, and had roughly 2 eV lower etching threshold energies. The etching threshold energy can be tuned by the film composition, making it possible to maximize the etching selectivity with respect to the gate and substrate materials. A generalized etch rate model was formulated based on the competing etching and depositing mechanisms involved in complex plasma chemistries, as determined from analysis of the experimental data , while the etch rate dependencies on neutral-to-ion flux ratio and ion energy were correctly represented. This surface site balance based approach accounts for competition between depositing and etching species with a steady-state overlayer, and employs proper assumptions for different chemistries at various energy regimes. The model fitted well to the experimental data under various ion energy and chemistry conditions, specifically, it was able to account for the transition between physical- and ion-enhanced etching in Cl_2 plasmas and the transition between deposition and etching in BCl_3 plasmas, as the ion energy increased. As quantitative information pertaining to high-k etching behavior can be extracted from this model, it is possible to extend its applicability to predict the etching characteristics of new materials in related plasma chemistries.

9:20am **PS-TuM5 Etch Challenges at the 22nm Node and Beyond**, ***R. Turkot***, Intel Corporation **INVITED**

As semiconductor manufacturing marches along according to its roadmap, the challenges of plasma etch at and around the transistor continue to increase. The last few generations have shown continued success to scale transistor gate lengths and simultaneously introduce novel transistor architectures with existing plasma etch technologies. Increasing numbers of new materials and continued scaling of material thicknesses and CDs promise to keep the pressure on plasma etch to deliver innovative solutions. Selectivities to multiple novel, thinner materials will be required. Etch tool environments may experience dramatic changes from traditional silicon or oxide etches and require "re-learning" of proper cleaning and conditioning. Even analysis of the structures being created becomes increasingly difficult as we march forward. Continued vigilance to the understanding of plasma etch and early identification of novel innovations to pattern, analyze and

sustain integrated solutions across research, development and manufacturing is paramount to the success of plasma etch at the 22nm node and beyond.

10:40am **PS-TuM9 Etch Mechanisms of Silicon Gate Structures Patterned in SF_6/CH_2F_2 Inductively Coupled Plasmas**, ***O. Luere***, Freescale Semiconductors, France, *L. Vallier, E. Pargon, O. Joubert*, LTM-CNRS, France

Patterning sub-40 nm gates presents several challenges among which maintaining a tight CD control is one of the most challenging. To succeed, understanding the etching mechanisms in gate patterning processes is one of the challenge. In this work we have investigated the different physical phenomena involved during the patterning of silicon structures in SF_6/CH_2F_2 based plasmas. The experimental work has been carried using a 200 mm etch platform connected, under vacuum, to an x-ray photoelectron spectroscopy surface analysis system. We have studied the impact of the SF_6/CH_2F_2 ratio on the silicon etch rate, thickness and composition of the reactive layer formed on the bottom silicon surfaces of the etched structures, thickness and composition of the sidewall passivation layer formed on the silicon sidewalls and silicon profiles. Our results demonstrate that there are very good correlations between the silicon etch rates and reactive layers formed on the bottom silicon surfaces. Contrary to previous studies performed using $HBr/Cl_2/O_2$ chemistries our results indicate that there is no simple correlation between the thickness of the CF_x passivation layer formed on the sidewalls and the final slope obtained in silicon. Our results demonstrate on the contrary, that even if very thin CF_x based passivation layers are formed on the silicon sidewalls, significant slopes can be generated in silicon. Other experimental results will be shown to elucidate the etch mechanism driving the silicon gate etch profiles during SF_6/CH_2F_2 plasma etching.

11:00am **PS-TuM10 Reduction of Si Recess during Gate Etching with RLSA Microwave Plasma Source**, ***T. Mori***, *M. Sasaki, T. Nishizuka, T. Nozawa*, Tokyo Electron Technology Development Institute, INC., Japan

As the design rule of ULSI devices continue to be scaled down, the critical dimension (CD) and reduction of silicon recess will need to be precisely controlled.[1] In this study, poly gate etching was evaluated to reduce silicon recess with RLSA (Radial Line Slot Antenna) microwave plasma source. RLSA generates plasma just below top dielectric plate, and as the plasma diffuses forward the wafer, its density and electron temperature become low immediately. The gate stack which was used for experiments consisted of SiN/Poly/Gate-Ox (2nm)/Si. First, it was etched with Vdc=-150V and Si recess was observed with TEM by changing over etching percent 50%, 100%, and 150%. The profile of gate stack was getting straight as increasing over etching percent and Si recess was less than 1.1nm. Second, by optimizing etching condition with lower Vdc=-135V, Si recess was 0.8nm and the profile kept straight. We suppose not only Vdc but also plasma potential Vp are effective factor to reduce silicon recess since the maximum ion energy can be estimated by adding plasma potential and Vdc. Comparing Vp under the same bias power between RLSA and RF plasma by ion energy analyzer on the chamber wall, it was found that RLSA plasma had lower Vp than RF one. RLSA can provide low Vdc and Vp condition keeping gate stack straight. This unique plasma characteristics will be able to use post 22 nm node Si etch like 3D gate that needs less etching damage on Si surface.

[1] S. A. Vitale and B. A. Smith, J. Vac. Sci. Technol. B 21, 2205 (2003).

11:20am **PS-TuM11 Effect of Inductively and Capacitively Coupled Plasma Pulsing on Charging of Features in Plasma Etching**, ***A. Agarwal***, *P.J. Stout, S. Banna, S. Rauf, K. Collins*, Applied Materials Inc.

Plasma charging damage presents challenges to maintaining critical dimensions during plasma etching of high aspect ratio (HAR) features (aspect ratio > 50). In one form of process induced charging damage, charge retention at the bottom of trenches can lead to breakdown as the accumulated charge stresses the material and creates a weak path for the injected current.[1] Charging damage occasionally manifests itself as tapering and twisting of HAR features, where the via or trench turns from the vertical to oblique direction.[2] This behavior is erratic in nature due to the randomness of the ion and radical flux composition as the feature dimensions approach only a few tens of nm. Polymer deposition on the sidewalls during dielectric etching can trap charge, which leads to less than ideal profiles. Neutral beam etching[3] (decreased interaction of charged particles with feature) and UV photon bombardment[4] (which increases surface current and conductivity allowing charge to drain through) have been suggested as useful techniques to mitigate charging damage. Pulsed plasma operation of an inductively or capacitively coupled plasma reactor may also allow for control of charging damage if negatively charged species can be extracted from the plasma. In this paper, pulsed and continuous plasma operations will be compared for etching in electronegative plasmas using results from a computational investigation. A 2-dimensional plasma equipment model (HPEM)[2,4] has been linked to a Monte Carlo feature profile model[5] to assess the consequences of pulsed plasma operation on charging of features. Results will be discussed for source and bias pulsing in an ICP reactor for poly-silicon etching and for pulsing of dual frequency CCP reactor for dielectric etching. Pulsed plasma operation allows for reduced interaction of charged species and depending on the mode of operation may allow for electrons to overcome the sheath potential thus neutralizing the accumulated charge. Sustaining a steady pulsed plasma can however be complicated in strongly electronegative gas mixtures as the plasma may not reignite after power is turned off.

[1] T. Ohmori and T. Makabe, Appl. Surf. Sci. 254, 3696 (2008).
[2] A. Agarwal, M.M. Wang, and M.J. Kushner, 54th AVS Symposium 2007.
[3] D.J. Economou, J. Phys. D 41, 024001 (2008).
[4] K. Rajaraman, Ph.D. Thesis, Univ. of Illinois (2005).
[5] P. Stout, 60th Gaseous Electronics Conference 2007.

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