Manufacturing Science and Technology
Room: 311 - Session MS+NC-MoM

CMOS Extension and Metrology
Moderator: V. Ku, TSMC

8:20am **MS+NC-MoM1 A Metal Hardmask Approach for the Contact Patterning of a 0.186 µm^2 SRAM Cell Exposed with EUV Lithography**, ***J.-F. de Marneffe***, *D. Goossens, A. Vandervorst, S. Demuynck, A.M. Goethals, J. Hermans, F. Van Roey, B. Baudemprez, S. Brus, C. Vrancken*, IMEC, Belgium

In order to overcome patterning challenges brought by dimensional scaling and aggressive pitches, extreme ultra-violet (EUV) lithography has been recently pushed forward as a possible solution for IC manufacturing, allowing extended exposure latitude at sub-50nm dimensions. This work address the technological solutions used for contact holes patterning by means of EUV lithography. A 0.186 µm^2 SRAM cell has been used as a test-vehicle, showing down to 55nm circular and boomerang-shaped contacts.[1] A metal hard-mask (MHM) approach has been selected, in order to combine the etch of high-aspect ratio features with thin EUV photoresist. The pre-metal dielectric stack covering the active fins was composed of 15nm Si_3N_4 as an etch-stop liner, covered by 240nm SiO_2. The MHM was made of a 30nm TiN film on top of which was spun 20nm of organic underlayer and 100nm of EUV photoresist. This paper will describe in details the various patterning steps (lithography, MHM opening and ash, SiO_2 followed by Si_3N_4 etch, residue cleaning) leading to the successful patterning of small contacts by EUV lithography.

[1] Imaging Performance of the EUV Alpha Demo Tool at IMEC, G.F. Lorusso et al., SPIE conference 6921-24 (2008).

8:40am **MS+NC-MoM2 Improved Mechanistic Understanding of Millisecond Annealing Techniques for Ultrashallow Junction Formation**, ***Y.V. Kondratenko***, *C.T.M. Kwok, E.G. Seebauer*, University of Illinois, Urbana-Champaign

Formation of pn junctions in advanced Si-based transistors employs rapid annealing techniques after ion-implantation in order to increase the electrical activation of dopants while minimizing their diffusion. Over the past decade, these techniques have evolved from rapid thermal processing, with time scales of about 1 s, to millisecond methods accomplished by flashlamps or lasers. Although the dopant behavior in terms of diffusion and electrical activation clearly improves as a result of the shortened time scale, the technology transition has taken place on a largely phenomenological basis with little understanding of the physical mechanism for the improvement. The present work provides the key elements of that understanding and explains nonthermal contribution of illumination on the diffusion of dopants. Continuum-based simulations were used to model experimental data in order to obtain mechanistic picture of improvement in dopant diffusion and activation during millisecond annealing. The same method was applied to explain photostimulated effects on dopant diffusion during soak annealing. The simulations solve the partial differential equations for diffusion and reaction of interstitial atoms, with activation energies for elementary diffusion and reaction steps computed by Maximum a Posteriori parameter estimation. The fundamental reason for improvements of diffusion and electrical activation in the millisecond regime is that the short time scale promotes exchange of dopant interstitial atoms with the lattice in preference to exchange with interstitial clusters. Photostimulated diffusion of dopants, however, exhibited more complicated features. Depending on annealing temperature and time, boron diffusion in silicon could be either enhanced or inhibited. Dopant activation was similarly affected. Simulations using continuum equations for the reaction and diffusion of defects were used to determine whether illumination affects cluster dynamics or steady state boron diffusion.

9:00am **MS+NC-MoM3 Challenges and Opportunities for 32nm Node CMOS and Beyond**, ***B. Doris***, IBM Research at Albany Nanotech **INVITED**

Future CMOS technologies require significantly more transistors per unit area with improved transistor performance. Gate-length, spacer, and contact scaling are the enablers for increasing transistor density. Scaling these features for future technology nodes is a significant challenge and new processes, materials and integration schemes will be needed. Ultimately new device architectures may be needed to achieve increased density or enhanced performance. Fully depleted SOI devices like Extremely Thin Silicon on Insulator (ETSOI) and FinFETs are the possible choices for alternate architectures. Either option would be a major shift for the semiconductor industry and would pose new challenges compared to conventional planar CMOS. Performance enhancement beyond previous technologies will be needed regardless of the particular device architecture choice. Recent experiments and simulation have shown that as the transistor density increases it is even more challenging to achieve similar performance. Specifically, recent technologies have relied on local mechanical stress techniques to enhance channel mobility and thereby improve performance. As the transistor density increases, the size of features and the distance between features decreases. This situation limits the ability of stress enhancement techniques to have impact on channel mobility. Thus, new performance elements are also needed for future technology nodes. This presentation highlights the opportunities and challenges for 32nm Node CMOS and beyond.

10:20am **MS+NC-MoM7 Multi Level "Air Gap" Integration for Advanced Technology Nodes**, ***F. Gaillard***, *D. Bouchu*, CEA-Leti-MINATEC, France, *R. Gras*, STMicroelectronics, France, *S. Moreau*, CEA-Leti-MINATEC, France, *G. Passemard, J. Torres*, STMicroelectronics, France

In order to extend device's performance and more particularly to improve interconnects RC delay, crosstalk and power consumption, continuous and innovative materials development have been realised over the twenty five past years to decrease dielectric constant. After the use of fluoride doped silicon oxide, low-k and later on porous ultra low k materials have emerged as serious candidates to isolate copper lines for the 90 - 32 nm nodes. Nowadays, "air cavities" introduction also named "Air Gap" represents the ultimate solution in this classical dielectric material evolution and is an attractive solution to meet the ITRS performance for advanced interconnects (22 nm technology node and below). We present an architecture where a sacrificial SiO_2 material deposited on few metal levels (two or more) is further removed by a hydrofluorhydric (HF) chemical etching agent. This HF chemistry diffuses through out patterned apertures localized in a silicon carbide (SiCN) capping layer deposited at the end of the multi level scheme. Thus, full air gaps realization is performed when possible, but SiO_2 pillars are still needed on long metal lines patterns to avoid any collapse when complete air cavities are made underneath. This global approach allows air cavities localization, keeps mechanical integrity and avoids any via misalignment issues, as air cavities are introduced at the end of the integration. In this work, we will present a three metal level interconnect realisation achieved at 65 nm design rules on a 300 mm diameter wafer; air cavities will be integrated on two metal levels and further completed up to pads realizations. Associated morphological and electrical results will be discussed. Based on simulation data and supported with experimental results, we have also predicted and demonstrated that an adequate stack composed of different doped or undoped SiO_2 materials deposited on the different metal levels can be useful to optimise the SiO2 pillar shape. It consequently improves the coupling capacitance gain on both metal levels, which is directly linked to the air cavities volume. Indeed, if the initial stack is composed of the same SiO_2 material, the air cavities present a spherical profile because the HF chemistry removes isotropically the SiO_2 layers through the specific apertures. These encouraging "Air Gap" results could represent a promising and low cost solution to move towards the next technology nodes.

10:40am **MS+NC-MoM8 Chemical Vapor Deposition of Manganese Self-Aligned Diffusion Barriers for Copper Interconnections in Microelectronics**, ***H. Kim***, *Y. Au, H. Wang, H. Bhandari, Y. Liu*, Harvard University, *D.K. Lee*, Samsung, *Y. Lin, R.G. Gordon*, Harvard University

Barriers to prevent diffusion of copper (Cu) and oxygen were formed by chemical vapor deposition (CVD) using a manganese (Mn) precursor vapor that reacts with silica-containing surfaces of low-k dielectrics. The manganese metal penetrates a few nanometers into the silica surface to make highly conformal, amorphous and insulating manganese silicate ($MnSi_xO_y$) layers on the walls of trenches and vias in interconnects. These $MnSi_xO_y$ layers were found to be excellent barriers to diffusion of Cu, oxygen and water. The adhesion of Cu to $MnSi_xO_y$ was also found to be sufficiently strong to satisfy the semiconductor industry requirements. The $MnSi_xO_y$ barrier/adhesion layers become part of the insulator structure, so that they maximize the space available for Cu in the trenches and vias. Thus $MnSi_xO_y$ is a "zero-thickness" barrier that exceeds the ITRS requirements for interconnections in future microelectronic devices. The same Mn CVD process can be applied to cap interconnect structures after chemical-mechanical polishing (CMP). On the tops of Cu wires exposed by CMP, the CVD process forms Mn that is initially dissolved in the Cu near its upper surface. During subsequent deposition of an insulator on the Cu, Mn diffuses back to the upper surface of the Cu where it forms a $MnSi_xO_y$ layer

that is strongly adherent to the Cu. These capping $MnSi_xO_y$ layers can increase the lifetime of interconnects against failure by electromigration.

11:00am **MS+NC-MoM9 What Photoemission Can Tell Us About High-K Dielectrics**, ***R.L. Opila***, *G. Liu*, University of Delaware **INVITED**
Angle-resolved photoelectron spectroscopy is an ideal probe films of candidate high dielectric constant films because the thickness of these very smooth films is comparable to the escape depth of the photoelectrons. We have successfully analyzed silicon oxynitride films of the range of thickness of 1 to 4 nm. From the N 1s spectrum we were able to identify four different binding states for N in these films: N bonded to three atoms: three silicon, two silicon and one oxygen atom, and one silicon and two oxygen atoms. In addition we identified a binding state corresponding to N bound to two silicon atoms with one unsatisfied, dangling bond. We also showed that converting the angle resolved data to a compositional depth profile could be done effectively using the maximum entropy algorithm. Recently we have been studying nitrided $(HfO_2)_x(SiO_2)_{1-x}$ films. The breadth observed in the N1s peak can be attributed to N binding to varying amounts of Si and the relatively electropositive Hf. There appears to be a tendency for N to preferentially bind to Hf in these films. We used the maximum entropy algorithm to analyze these films. Nitridation at successively higher temperatures results in more incorporation of N into these films, and more of this N is incorporated near the oxide/Si interface. Using maximum entropy we were able to convert the angle resolved data to compositional depth profile that had adventitious oxide on the surface, preferential oxidation at the outer surface and the oxide/silicon interface, and otherwise relatively smooth composition of Si^{+4} and Hf^{+4} through the film. These results were confirmed qualitatively by medium energy scattering.

11:40am **MS+NC-MoM11 Influence of Room Temperature Control System on AFM Imaging**, ***J. Fu***, National Institute of Standards and Technology, ***W. Chu***, Harbin Institute of Technology, China, ***T. Vorburger***, National Institute of Standards and Technology
As the technology progresses, the control of the thermal and vibrational environment for experiments is also becoming more sophisticated. In particular, temperature control to within ± 0.25° C for a general purpose lab is fairly common place. However, even with such a stringent temperature control specification, the variation of temperature can be observed in the AFM (atomic force microscopy) images of a straight edge. In this paper we show the correlation between edge distortion of a semiconductor linewidth standard and the thermal recycling in the lab imposed by a two-level infrastructural temperature control system. A Fast Fourier Transform (FFT) analysis of the AFM images of the line links the frequency of the waviness at the line edge to the damper and reheating coil of the air conditioning feedback system. The unique frequency components present in all three axes of AFM images lead us to conclude that the temperature variation affected the PZT scanner which affected the measurements.

Authors Index

Bold page numbers indicate the presenter