Electronic Materials and Processing
Room: 210 - Session EM-WeM

High-K Oxides and High Mobility Substrates

Moderator: R.M. Wallace, University of Texas at Dallas

8:00am **EM-WeM1 Spectroscopic Detection of Conduction Band Edge Defects in HfO_2, Hf Si Oxynitride and Stacked Hf Si Oxynitride/HfO_2 High-k Dielectrics: Extraction of Defect States from O K Edge NEXAS Spectra**, *K.B. Chung, H. Seo, J.P. Long, G. Lucovsky*, North Carolina State University

A novel approach for eliminating Ge-N bonding at Ge-high-k dielectric interfaces from sacrificial Ge nitride interfacial transition regions (ITRs) used to passivate the Ge substrate against oxidation during film deposition. The GeN ITRs can be effectively eliminated during an 800°C post-deposition one minute anneal in Ar leaving the HfO_2 films in direct bonding contact with Ge(100) or Ge(111) substrates. This paper presents a study of band edge electronic structure, including band edge defects as function of annealing temperature by comparing near edge X-ray absorption spectra (NEXAS), O K_1 and N K_1 edges, for films deposited on a ~0.6-0.8 nm interfacial Ge-N layer, and after partial and complete removal of interfacial Ge-N and/or Ge-O bonding for anneals up to 800°C in Ar. Three types of dielectrics have been addressed: i) HfO_2, ii) high Si_3N_4 content Hf Si oxynitride alloys, and iii) stacked dielectrics comprised of high Si_3N_4 content Hf Si oxynitride alloy/HfO_2. One of the primary sources of defects in the HfO_2 films is associated with the incorporation of Ge, which has been detected in SXPS/UPS spectra. Finally defects identified in HfO_2 spectroscopically, explain large differences in the tunneling currents.

8:20am **EM-WeM2 ARXPS Study of the Early Stages of the Formation of the HfO_2/Si and HfO_2/SiO_2 Interfaces**, *M.D. Morales-Acosta, A. Herrera-Gomez*, Cinvestav-Unidad Queretaro, Mexico, *F.S. Aguirre-Tostado, J. Kim, R.M. Wallace*, The University of Texas at Dallas

The interfacial layer that is formed as hafnium oxide is deposited on silicon affects the performance of hafnium-based C-MOS devices. Although the composition of the interfacial layer could be evaluated from electrical measurements,[1] a more direct approach is desirable. The ideal technique for this type of studies is ARXPS because of its unparallel chemical and depth resolution. We performed high resolution ARXPS studies on ALD HfO2 film grown on H-terminated and 1nm SiO2-terminated Si(001) surfaces employing 5 and 30 cycles (H2O and TEMA-Hf). The deconvolution of the peaks was done robustly. Since surface potentials could also cause "chemical" shifts on the binding energies, the physical origin of the different peaks was assigned not only from the peak position but also from the detailed analysis of the take-off angle dependence of the peak area. It was possible to learn about the early stages of the HfO2/SiO2 interface formation since the thickness of the hafnium oxide layer for the samples with 5 ALD cycles were less than one monolayer. Although the 30 cycle ALD growth resulted in stoichiometric 2nm HfO2 films for both surfaces, in the early stages the growth of the HfO2 was more efficient for the SiO2-terminated sample. The first ALD cycles in the H-terminated samples caused the formation of 1.5ML of oxidized silicon. The Si 2p binding energy was 102.9eV, 0.4eV smaller than for the SiO2-terminated samples. Our analysis shows that this difference could be associated to the known dependence of the Si 2p binding energy on the oxide growing process, and not to the formation of a hafnium silicate layer for the H-terminated surfaces. As reported elsewhere,[2] there is a component (Hf*) with Hf 4f binding energy 0.6eV higher than for hafnium oxide. The analysis strongly suggests that Hf* could be associated to the first layer of HfO2 in contact with the SiO2, and not to a hafnium silicate layer. We concluded that the ALD process produced an abrupt SiO2/HfO2 interface, even for the H-terminated samples. A clear description of the self-consistent ARXPS analysis will be presented. This work was supported by the Semiconductor Research Corporation and the Texas Enterprise Fund.

[1]S. K. Dey, A. Das, M. Tsai, D. Gu, M. Floyd, R. W. Carpenter, H. De Waard, C. Werkhoven, and S. Marcus. J. Appl. Phys. 95, p. 5042 (2004).
[2]N. Barrett, O. Renault, J.F. Damlencourt, and F. Martin. J. Appl. Phys. 96, p. 6362 (2004).

8:40am **EM-WeM3 Characterization of High-k Dielectric and Metal Gate Film Stack by AR-XPS**, *G. Conti, Y. Uritsky, C. Lazik, S. Hung, N. Yoshida, M. Agustin, X. Tang, R. Wang*, Applied Materials Inc.

The implementation of a higher-k hafnium-based dielectric coupled with an atomically engineered oxynitride interface addresses gate leakage while maintaining high mobility. In conjunction with the new dielectric stack, metal gates are replacing polysilicon gate electrodes for material compatibility and performance. Devices made with high-k/metal gates can achieve >100x improvement in gate leakage, with significantly greater switching speed. The desirable properties of the dielectric High-K layer are : high dielectric constant; low leakage current; and thermal stability against reaction or diffusion to ensure sharp interfaces with both the substrate Si and the gate metal . Extensive characterization of such materials in thin-film form is crucial not only for the selection of alternative gate dielectrics and processes, but also for the development of an appropriate metrology of the high-k films on Si. This paper will report recent results on structural and compositional properties of Al2O3 deposited on 20A ALD HfO2 / 8A SiO2 . This stack was capped with 20A TiN . Angle-resolved XPS showed that after the high temperature anneal Al diffused into the dielectric stack with its concentration peaking at the HfO2/SiO2 interface and some remaining at the HfO2 surface. No Al was detected near the Si substrate interface suggesting that the insertion of Al2O3 cap layer at the high-k/metal gate interface and subsequent high temperature process should not degrade the device channel mobility. The AR-XPS and the TEM results are compared to the electrical data.

9:00am **EM-WeM4 Density-Functional Theory Molecular Dynamics Simulations of a-Al_2O_3/Ge(100)(2x1), a-Al_2O_3/$In_{0.5}Ga_{0.5}As$, a-Al_2O_3/$In_{0.5}Al_{0.5}As$/$In_{0.5}Ga_{0.5}As$**, *E. Chagarov, A.C. Kummel*, University of California, San Diego

Amorphous oxide-semiconductor interfaces are keys to the performance of all metal-oxide field effect transistors (MOSFETs), but little is known about the exact bonding geometry at the interface. In this study, the bonding of a single amorphous oxide onto three semiconductors is compared to understand selective bond formation and intermixing since interfaces with non-polar bonds, no intermixing, and no half-filled dangling bonds are optimal for MOSFET devices. The local atomic and electronic structure of a-Al_2O_3/Ge(100)(2x1), a-Al_2O_3/$In_{0.5}Ga_{0.5}As$, and a-Al_2O_3/$In_{0.5}Al_{0.5}As$/$In_{0.5}Ga_{0.5}As$ interfaces were investigated by density-functional theory (DFT) molecular dynamics (MD) simulations. Realistic amorphous a-Al_2O_3 samples were generated using a hybrid approach including classical and DFT molecular dynamics. Each amorphous oxide/semiconductor interface was formed by placing an amorphous oxide sample on a slab of one of the semiconductors and annealing the stack at 700K / 800K and 1100K; subsequently, the stack was cooled and relaxed to get the final oxide-semiconductor interfacial bonding structure. The a-Al_2O_3/Ge interface demonstrates strong chemical selectivity with Al atoms migrating out of interface into the oxide bulk and O atoms migrating into the interface region resulting in interface bonding exclusively through Al-O-Ge bonds creating a large interface dipole; this exclusive Al-O-Ge bonding is due to Al-O bonds being more energetically favorable than Al-G bonds. During annealing of a-Al_2O_3/$In_{0.5}Al_{0.5}As$/$In_{0.5}Ga_{0.5}As$, Al migrates from InAlAs to a-Al_2O_3, demonstrating interfacial mixing; the intermixing is driven by the high energy of formation for Al-O bonds. The a-Al_2O_3/$In_{0.5}Ga_{0.5}As$ interface has polar As-Al bonds and In/Ga-O bonds of opposite dipole direction, low lattice distortion, and no intermixing. The formation of two types of bonds with opposite dipoles is driven by electronegativity: Al, an electron donor, bonds to As an electron acceptor while O, an electron acceptor bonds to In/Ga, electron donor.

9:20am **EM-WeM5 Atomic Layer Deposition (ALD) of Amorphous High-k Dielectric Films of $La_{(1-x)}M_xO_{3/2}$, M = Al, Sc, Lu, Y and La**, *H. Wang, M. Coulter, Y. Liu, J.J. Wang, R.G. Gordon*, Harvard University, *J.S. Lehn, H. Li, D.V. Shenai*, Rohm and Haas Electronic Materials

ALD was used to deposit films containing lanthanum and other trivalent elements aluminum, scandium, lutetium and yttrium. The precursors are N,N'-dialkylformamidinates or acetamidinates, except for aluminum, for which trimethylaluminum was used. The oxygen source was water vapor, which was sometimes supplemented with molecular oxygen to eliminate oxygen vacancies. Substrates used include silicon, germanium, gallium arsenide, ruthenium and titanium nitride. The films are amorphous as deposited, and have no interfacial layer between the dielectric an silicon. The films remain amorphous after rapid thermal annealing to temperatures as high as 1000 ºC. High dielectric constants and very low leakage currents were measured. Dielectric constants remain the same even when the film thickness is reduced to ~ 5 nm, leading to EOT values < 1 nm with leakage currents < 10^{-3} A cm^{-2}.

9:40am **EM-WeM6 Boron Oxynitride as Gate Dielectric Films for Future CMOS Technology**, *N. Badi, S. Vijayaraghavan, A. Bensaoula*, University of Houston, *A. Tempez, P. Chapon*, Horiba Jobin Yvon, France, *N. Tuccitto, A. Licciardello*, University of Catania, Italy

Existing silicon oxynitride dielectric can only provide a very near term solution for the CMOS technology. The emerging high-k materials have a limited thermal stability and are prone to electrical behavior degradation

which is associated with unwanted chemical reactions with silicon. We investigate here applicability of amorphous boron oxynitride (BO_xN_{1-x}) thin films as an emerging high temperature gate dielectric. (BO_xN_{1-x}) samples of thickness varying from 10 nm down to 1 nm were deposited in a high vacuum reactor using filamentless ion source assisted physical vapor deposition technique. The (BO_xN_{1-x}) dielectric structural and mechanical properties were investigated as a function of thickness and O/N composition. B10 implanted (BO_xN_{1-x}) /Si heterostructures and (BO_xN_{1-x}) layers deposited on B10 implanted Si substrates were post annealed at high temperatures up to 1000°C. Depth profiling of these layers were performed to evaluate the stability of the dielectric layers and their efficacy against B dopant diffusion simulating processes occurring in activated polySi-based devices. Elemental composition along with chemical and electronic states analysis of the layers were carried out using Secondary Ion Mass Spectrometry (SIMS), Glow Discharge Optical Emission Spectroscopy (GDOES), Glow Discharge Time of Flight Mass Spectrometry (GD-TOFMS) and X-ray Photo-Electron Spectroscopy techniques. Preliminary results show that (BO_xN_{1-x}) dielectric constant ranges from 4 – 6 and that capacitance change with temperature (25°C- 400°C) and frequency (10 KHz-2 MHz) is about 10% and 2%, respectively. Our conclusions on suitability of (BO_xN_{1-x}) for advanced energy storage devices and gate dielectric for future CMOS technology will be presented.

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10:40am **EM-WeM9 Electrical and Physical Properties of High-k Gate Dielectrics on III-V Semiconductors**, ***E.M. Vogel***, *C.L. Hinkle, A. Sonnet, F.S. Aguirre-Tostado, M. Milojevic, K.J. Choi, H.C. Kim, J.G. Wang, H.C. Floresca, J. Kim, M.J. Kim, R.M. Wallace*, The University of Texas at Dallas **INVITED**

Because of a significantly higher electron mobility compared to silicon, III-V semiconductors (e.g. GaAs, InGaAs) with high-k gate dielectrics (e.g. Al_2O_3, HfO_2) are being considered for future Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). However, device performance has been limited by high electrically active interfacial defect density. Various physical characterization techniques including monochromatic x-ray photoelectron spectroscopy (XPS) and high-resolution transmission electron microscopy (HRTEM) are used to study the physical properties of atomic-layer-deposited Al_2O_3 and HfO_2 dielectrics with various interlayers (e.g. silicon), precursors and surface treatments. Characterization and modeling of the electrical properties of MOS capacitors and MOSFETs is correlated to the details of the bonding arrangements and physical properties of the dielectric stacks. The results suggest that proper selection of interlayer, ALD precursors, and surface treatment can result in selective interfacial bonding arrangements and associated device electrical properties.

11:20am **EM-WeM11 Surface Structure and Fermi Level Determination of Oxides/III-V Interface**, ***J. Shen***, *A.C. Kummel*, University of California, San Diego

We have used scanning tunneling microscopy (STM) and density functional theory (DFT) calculations to both identify the group III rich III-V surface reconstruction and to identify the bonding structure for oxide on these surfaces. In-rich InAs(001)-(4×2) can readily be prepared by decapping of As2 capped InAs(001) wafers. STM results reveal that In-rich InAs(001)-(4×2) has a very different atomic structure than Ga-rich GaAs(001)-ζ(4×2) structure even though the surfaces have similar symmetry. The InAs(001)-(4×2) is denoted as the β3(4×2) and has a unit cell consisting of two undimerized group III atoms on the row and two group III dimers in the trough. STM results showed that the initial deposited In2O molecules bond to the edges of the rows and most likely form new In-As bonds to the surface without any disruption of the clean surface structure. Annealing the In2O/InAs(001)-(4×2) surface at 400˚C results in formation of flat order monolayer rectangular islands onto which oxide grows in a layer-by-layer mechanisms with amorphous structure. In0.53Ga0.47As is a good candidate for a III-V MOSFET due to its high carrier mobility, low density of thermal carriers, and ability to be grown lattice matched on semi-insulator InP substrates. STM images of the clean surface indicate that the In0.53Ga0.47As(001)-(4×2) surface reconstruction is similar to the InAs(001)-(4×2) structure. The DFT calculations reveal that the some of the trough dimers are buckled, which is consistent with the STM images showing that the trough has poor order. Ga2O was deposited on the surface to determine how oxide adsorbates bond to In0.53Ga0.47As(001)-(4×2) clean surface. The bonding structure of the annealed Ga2O/In0.53Ga0.47As(001)-(4×2) is similar to that of In2O/InAs(001)-(4×2); however, the Ga2O/ In0.53Ga0.47As(001)-(4×2) islands are more weakly ordered than the In2O/InAs(001)-(4×2) islands. For both In2O/InAs(001)-(4×2) islands and Ga2O/ In0.53Ga0.47As(001)-(4×2), the oxide adsorbates never cause the abstraction of any surface atoms on the InAs and In0.53Ga0.47As(001)-(4×2) surfaces; furthermore, for monolayer oxide films, the oxide molecules only occupied specific sites. After high temperature annealing, the oxide desorbs from the surface and the clean (4×2) surface is restored. This is consistent with the formation of a smooth interface between the oxide and the semiconductor.

11:40am **EM-WeM12 High-K Dielectrics/High Mobility Channel Interface Optimization for Future CMOS Technology**, ***L. Yu***, *T. Feng, Q. Jiang, H.D. Lee, C.L. Hsueh, A.S. Wan, D.D.T. Mastrogiovanni, Y. Xu, T. Gustafsson, E. Garfunkel*, Rutgers, The State University of New Jersey

High-k dielectrics have been adapted as gate oxide in order to prolong the Moore's law of CMOS transistor scaling to a critical length of 45 nm and beyond. Also, replacing Si with a higher mobility material (for example, Ge and III-Vs) as transistor channel is expected to further enhance the transistor performance. Thus, the idea of combining those two advances in one process has attracted many research efforts from both academia and industry. However, the task has been difficult due to the lack of proper treatment to the oxide/channel interface. The defect states at the interface or inside dielectrics can enhance carrier scattering and degrade device threshold voltage. Further more, the chemical instability and compatibility at the interface are often detrimental to device performance. Several studies, including ours, showed that chemical cleaning and subsequent passivation (for example, with ammonium sulfide) prior to dielectrics deposition on both Ge and GaAs channels can greatly reduce the interface state density (Dit). We have established tools that enable ALD and sputtering deposition of the CMOS gate stacks along with in.situ. characterization by MEIS (Medium Energy Ion Scattering) and XPS. It allows us to determine, with high spatial resolution, the composition, structure and thermal stability of gate stacks on various channels. We will present the in. situ. characterization results of Al2O3 and HfO2 based gate stacks on chemically treated Ge and GaAs surface. These results will be directly correlated with studies of gate stack electrical properties and electronic structure.

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