Plasma Science and Technology

Room: 607 - Session PS2+MS-MoM

Plasma Etching for Advanced Interconnects I

Moderator: V. Ku, Applied Materials

8:00am **PS2+MS-MoM1 Challenges for Microwave Plasma Etching of Low-k Dielectrics**, ***T. Nozawa***, *M. Inoue, T. Nishizuka*, Tokyo Electron LTD Japan **INVITED**

Meeting post 32 nm etch process integration requirements with porous SiCOH and conventional plasma sources is a challenge as the SiCOH surface is decomposed by reactions induced by electron, ion, radical and UV radiation exposure. This exposure is inherent to most plasma systems making it difficult to achieve both high precision and damage free etching. Neutral beam etching has been developed to provide ion and UV radiation free and therefore damage free etching processes. Neutral beam etching by itself lacks the benefits of energy and chemistry control afforded by in-situ plasma processes. A Radial Line Slot Antenna (RLSA) driven surface-wave-plasma at 2.45GHz generates very high density plasma with high electron temperature in a region limited to just below the dielectric plate through which microwave pass. Both chemistry and energy control are achieved with the RLSA configuration. Plasma is transported to the wafer by diffusive transport through a low electron temperature region. An electronegative precursor gas (e.g., C4F8) is injected into the low electron temperature region so that dissociation is not excessive and a substantial negative ion population is generated near the wafer. An RF bias frequency 400kHz through the wafer provides ion acceleration without plasma generation. The combination of the low electron temperature electronegative downstream plasma with the low driving frequency facilitates charge damage free etching for all process conditions. Another consequence of the combination of plasma conditions near the electrode is that physical damage of SiCOH material is eliminated and k-value increase is minimized. This is achieved through dissociation control which results in the population reduction of small very reactive species such as H* and F* and the retention of sidewall polymer integrity. The unique plasma characteristics of the RLSA system will be described in this presentation with an emphasis on process performance for post 32 nm node CMOS fabrication.

8:40am **PS2+MS-MoM3 High Frequency Capacitively Coupled Plasma for Low Ion Energy Dual Damascene Etching**, ***A. Marakhtanov***, *E.A. Hudson, K. Takeshita, O. Turmel*, Lam Research Corp.

Capacitively coupled discharges are widely used for semiconductor processing, especially in the area of dielectric etching. With a wide range of film materials and complex stacks including multiple mask layers, advanced dielectric etch processes require tight control of plasma parameters, such as ion flux, radical composition, and ion energy distribution (IED). This paper presents IED measurements and patterned-wafer etch results as a function of RF bias excitation frequency applied to the wafer electrode. The aim is to produce the optimal IED for etching of soft materials, such as low-k dielectrics commonly used in Dual Damascene interconnect schemes. One key challenge arises in the trench etch step, which requires a vertical etch profile in the low-k film. But the process must avoid corner faceting of any exposed via holes or of the hard mask layer which defines the initial trench pattern. Faceting would cause an increase in via or trench critical dimension, respectively. The competing requirements of vertical profile and minimal faceting define a fairly narrow range of acceptable ion energies for the process. If power is held constant, higher RF driving frequencies typically produce plasmas with higher densities and lower potentials, and enable operation at lower pressure. Both the mean ion energy and width of the IED reaching the wafer tend to decrease as the wafer bias frequency increases. For frequencies too low, the width of the IED is too large and faceting is induced by the high energy ions. For frequencies too high, the mean IED is too low to etch the low-k film with a vertical profile and acceptable rate. Results show that the necessary IED for these applications can be obtained by applying 60MHz to the wafer electrode.

9:00am **PS2+MS-MoM4 Energy Distribution of Bombarding Ions, Etch Selectivity and Profile Control in Plasma Etching of Dielectrics**, ***F.L. Buzzi***, *Y.-H. Ting, A.E. Wendt*, University of Wisconsin-Madison

The energy distribution of bombarding ions during plasma etching of dielectrics for microelectronics manufacturing affects both selectivity to photoresist and the profile shape of the etched feature. Here we examine the role of ion bombardment making use of an ability to produce either a narrow ion energy distribution (IED) at a specified energy, or a two-peaked distribution in which the energy and relative flux of the two peaks can be controlled. A system has been developed for manipulating the IED at the substrate during plasma etching by controlling the voltage bias waveform of the RF bias applied to the substrate. The output of a waveform generator drives a broadband power amplifier connected to the electrode, and is programmed in an iterative process to produce the desired substrate wave form. The iterative feedback process has recently been automated so that arbitrary waveforms can be quickly achieved. Waveforms to produce ions at the substrate with energies greater than 500 eV in single-peaked or two-peaked IEDs are now routinely produced, and are applied to etching of silicon dioxide in fluorocarbon-based gas mixtures. Prior studies with a single-peaked IED at energies below 200 eV showed significant improvements in etch selectivity compared to a sinusoidal bias producing a broad IEDF (Wang and Wendt, 2001, Silapunt et al., 2003). In this study, we will report on a systematic characterization of IED effects on blanket and patterned wafers. Results include the following: 1) effect of ion energy on photoresist and oxide etch rates for the narrow single-peaked IED at high energy, 2) effect of ion energy on photoresist roughening/distortion, to explore evidence of improved performance with higher energy ions, and 3) systematic study of the asymmetric bimodal IEDs as a function of the relative ion fluxes at the two energies, to examine the effect on etch rates for oxide and photoresist and etched feature profiles. The plasma system is equipped with a helicon plasma source operating at 13.56 MHz. The substrate electrode accommodates 4" diameter wafers, and is equipped with helium backside cooling and a thin film laser interferometer to monitor etch rates of blanket films. The chamber walls are heated externally to minimize process drift associated with wall temperature changes during plasma operation.

9:20am **PS2+MS-MoM5 Etch Plasma Chemistry and Film Variability Effects on Dual Damascene Patterning of Porous Ultra-low k Materials**, ***C.B. Labelle***, AMD, Inc., *J. Arnold*, IBM Research, *H. Wendt*, Infineon Tech., *R.P. Srivastava*, Chartered Semicon. Mfg Ltd., *K. Kumar, Y. Choi, H. Yusuff, S. Molis, C. Parks, C. Dziobkowski, M. Chace, A. Passano, L. Tai*, IBM Microelectronics, *D. Kioussis*, AMD, Inc., *J. Yamartino, D. Restaino, L. Nicholson*, IBM Microelectronics

Porous ultra low k dielectrics ($k < 2.5$) are being integrated into current and future technology nodes. A large focus of the integration of these films has been on the sensitivity of the films to compositional modification (i.e., carbon depletion) during resist strip in the dual damascene patterning scheme. As porous ultra low k dielectric strip processes have evolved and matured, new sensitivities have emerged which affect successful integration. This paper will discuss a case where, in a via-first-trench-last dual damascene integration scheme, the plasma chemistry used during via etch has been found to affect the profiles after trench etch when etching porous ultra low k dielectrics ("ULK via/trench interaction"). Modifications to the via etch plasma chemistry can be made to bring the trench profile back to target, but repeatability of the success of these workarounds is key. Variability in the film composition through the bulk of the film can also instigate post-etch profile changes or exacerbate the etch plasma-induced via/trench interaction. Data will be shown demonstrating the sensitivity of the etch processes to film composition variability. Possible mechanisms for the ULK via/trench interaction will also be discussed.

9:40am **PS2+MS-MoM6 Surface Roughening Mechanisms during Porous SiOCH Etching Processes**, *F. Bailly*, CNRS/IMN - France, ***T. David***, CEA/LETI-MINATEC - France, *T. Chevolleau, M. Darnon*, CNRS/LTM - France, *C. Cardinaud*, CNRS/IMN - France

Introducing dual damascene structures for the interconnections has been a means of improving their electrical performances. However, lowering the effective dielectric constant remains a major stake. Increase the porosity of the dielectric material or remove the trench bottom etch stop layer are some solutions. As a result, the trench etch process is stopped into the porous material which may lead to a tricky trench bottom roughness. In addition, sidewall metal diffusion barriers have to be thinned down to keep the copper line resistance low. In this context, the trench bottom roughness may also affect metal barrier coverage. In this study, roughness of dielectric materials is characterized by SEM and AFM after partial etching. Dielectric etching is known to be controlled by the thickness and composition of a fluorocarbon overlayer which depends on the plasma characteristics (etch chemistry…) and on the materials properties (composition, porosity,…). Thereby, in order to understand the mechanisms controlling the porous SiOCH roughening, different etch plasmas have been performed on materials with different percentages of porosity (7, 25 and 30%). For a high polymerizing ($CF_4/Ar/CH_2F_2$), a low polymerizing (CF_4/Ar) and a pure

physical sputtering plasma (Ar), surface composition has been characterized by quasi in situ XPS and the roughness has been studied as a function of the etched thickness. Those experiments highlight different trends. Firstly, the 7 % porous SiOCH does not exhibit any significant roughness whatever the etching plasma (rms roughness = 0.5nm). Secondly, porous SiOCH with a higher porosity (25 and 30%) is roughened when exposed to fluorocarbon based plasmas. The resulting roughness increases linearly versus the etched thickness in the range of a tenth of nanometers. This increase is fast when the concentration of fluorocarboned species at the etched surface is low, while a higher amount of fluorocarboned species limits it. At last, sputtering of porous SiOCH using a pure Ar plasma, namely the absence of fluorocarboned species at the etched surface, leads to a surface as smooth as the pristine material (rms roughness = 0.2 nm). Those results highlight the critical role of porosity and the presence of fluorocarboned species on the dielectric surface roughening. On the basis of those observations, a hypothesis will be proposed for the initiation and maintaining of the dielectric roughness.

10:20am **PS2+MS-MoM8 Design for Manufacturability through Design-Process Integration**, ***A. Neureuther***, University of California, Berkeley **INVITED**

Exploratory prototype Design for Manufacturing (DFM) tools and methodologies are described. Examples will include new platforms for collaboration on process/device/circuits, visualization/quantification of manufacturing effects at the mask layout level, and fast/approximate physical modeling for first-cut design decisions. The examples have evolved from research supported over the last several years by DARPA, SRC, Industry and the U.C. Discovery Program on aberrations, illumination, polarization, CMP, plasma etching and device variation. DFM tools must enable complexity management with very fast approximate models across process, device and circuit performance with new modes of collaboration. Circuit Designers have good complexity management skills can add value by participating in this collaboration. Collaborations can be promoted by supporting multiple views of the trade-offs in terms of the natural intuitive parameters of each collaborator. Many of the nonidealities of manufacturing can be expressed at the mask plane in terms of lateral impact functions. This allows visualization and quantitative assessment of effects that are not easily captured even with large sets of design rules. Pattern Matching and Perturbation Formulation have promising exceptional speed and adequate accuracy for implementing these lateral impact assessments.

11:00am **PS2+MS-MoM10 Feature Profile Simulation for Organic Low-k Etching in 2f-CCP in H_2/N_2**, ***T.Y. Yagisawa***, *T. Makabe*, Keio University, Japan

As the size of ULSI continuously shrinks up to 45 nm in 2010 and multi-layer interconnect with more than 12 layers is applied, RC (resistance-capacitance) signal delay should be made smaller to meet the demand for higher performance of signal transmission. The dielectric constant of interlayer dielectric (ILD) can be reduced by lowering electric polarizability of the material. Alternatively introducing nano-holes within the material to reduce its density, decreases the k value. Increasing porosity is considered as a promising candidate for obtaining low-k ILD, though it may bring up new serious problems in its processing. Materials with low dielectric constant tend to possess poor mechanical strength and adhesiveness to the wire. In addition, low-k dielectric has low heat conductance and low resistance against heat, which makes it difficult to go through the post annealing in back-end processes. Currently, H_2/N_2 plasma is developed as the most suitable tool for the etching of organic low-k material. The etching profile is determined under the balance among isotropic etching by reactive H radical, physical sputtering by energetic ions and surface protection by the deposition of N radical. In order to attain the optimal profile, detailed understanding of these elements throughout the whole plasma etcher is strongly required. We have developed an integrated simulation consisting of the flux-velocity distribution of reactive species and the feature profile evolution of organic low-k etching in two frequency capacitively coupled plasma (2f-CCP) in the admixture of H_2/N_2.[1] In the present study, we will first estimate the density of reactive species, such as H, N and NH_x radicals, generated mainly via direct dissociation from parent gas molecules. Further, the effect of dissociation degree on the etching profile will be discussed as a function of the mixture ratio of feed gases.

[1]K. Ishihara et. al., Plasma Physics and Controlled Fusion, 48, B99 (2006).

11:20am **PS2+MS-MoM11 Removal of Scallops formed during Deep Via Etching for 3D Interconnects**, ***Y.-D. Lim***, *S.-H Lee*, *C.-H. Ra*, *W.J. Yoo*, Sunkyunkwan University, Korea

Three dimensional (3D) integration using chip-to-chip interconnects is currently receiving great attention since it can bring about substantial advantages in high packing density, low power consumption and high speed operation over planar circuits integration. Deep etching of high aspect ratio vias is known be the most critical step to realize the 3D interconnects. When the Bosch process which alternately introduces SF6 for isotropic etching and C4F8 for sidewall passivation is implemented to form deep via holes, the formation of scallops along the sidewall is unavoidable and poses a serious obstacle to scale down design rule in this scheme. In this work, we investigated methods to remove scallops using post O2 based plasma treatment assisted by subsequent HF based wet etching treatment, when inductively-coupled plasma etching had been applied to form various via hole sizes down to 2.5um with depths up to 100um. According to the experimental results, the removal of scallops was dependent on the via hole size, the orientation of scallop directed out of the sidewall, the combination of the post plasma etching chemistry and the subsequent wet etching chemistry, and the profile of etched structure. Furthermore, it was found that the removal of scallops is more effective for vias of larger and for more vertical structures. The technology developed in this work was proven to be suitable for subsequent electroplating of Cu interconnects.

11:40am **PS2+MS-MoM12 High-rate Deep Anisotropic Silicon Etching with the Expanding Thermal Plasma Technique**, ***M.C.M. van de Sanden***, *M.A. Blauw*, Eindhoven University of Technology, Netherlands, *F. Roozeboom*, NXP Semiconductors Research, *W.M.M. Kessels*, Eindhoven University of Technology, Netherlands

Emerging microsystem and 3D interconnect technologies require high anisotropic etch rates to accommodate Si etch depths exceeding 200-300 μm and aspect ratios higher than 10. Using inductively coupled plasma (ICP) reactors there has been a steady improvement of the performance of deep anisotropic Si etching, however, it is unclear whether sufficiently high etch rates can be obtained by continuous innovation of the existing ICP technology. Following our work on high-rate deposition of a wide variety of materials, we have explored deep anisotropic Si etching with the expanding thermal plasma (ETP) technique using fluorine-based chemistries. The ETP technique consists of a remote high-density plasma source and due to a low downstream electron temperature (< 0.3 eV) it has a good control of the plasma chemistry and ion energy. Both a cryogenic etching process and a time-multiplexed etching process were developed using SF_6-O_2 and SF_6-C_4F_8 etch chemistries, respectively. The ion energy was controlled by employing several substrate biasing schemes, including rf and pulse-shape biasing. In this contribution we will present data on etch rates, anisotropy, and selectivity with regard to the hard mask and it will be demonstrated that etch rates up to 12 μm/min and selectivities higher than 300 can be obtained by the ETP technique. Insight in feature profile control will also be presented and it will be shown that feature profiles are comparable to those obtained with ICP reactors. This novel, ETP-based deep anisotropic silicon etching technique might therefore be an attractive alternative for the fabrication of silicon microstructures with high-aspect-ratio features.

Nanometer-scale Science and Technology

Room: 616 - Session NS+MS-TuA

Characterization of Nanostructures

Moderator: R.F. Klie, University of Illinois - Chicago

1:40pm **NS+MS-TuA1 Atomic-scale Deformation in N-doped Carbon Nanotubes**, ***C.-L. Sun***, Academia Sinica, Taiwan, *H.-W. Wang, M. Hayashi, L.-C. Chen,* National Taiwan University, *K.-H. Chen*, Academia Sinica, Taiwan

We present the N-doping induced atomic-scale structural deformation in N-doped carbon nanotubes (CNTs) by using energy-filtered transmission electron microscopy (EFTEM) and density functional theory calculations. EFTEM N mapping image shows that N is indeed incorporated in the bamboo-like CNTs with non-uniform distribution. The interlinked parts in CNTs are brighter than the sidewall, indicating that they contain higher N concentration. We then construct the finite cluster models for CNTs with pure and two doping types in order to study the detailed structural changes in atomic scale. For substitutional-N-doped nanotube clusters, the N dopant with an excess electron lone pair exhibits the high negative charge and the homogeneously-distributed dopants enlarge the tube diameter in both zigzag and armchair cases. On the other hand, in pyridine-like-N-doped ones, the concentrated N atoms result in positively curved graphene layer and thus can be responsible for tube wall roughness and the formation of interlinked structures. Several examples for its relevant applications in energy conversion and storage will be briefly introduced in the end.

2:00pm **NS+MS-TuA2 Four-Tip Scanning Tunneling Microscope for Measuring Transport in Nanostructures**, ***S. Hasegawa***, University of Tokyo, Japan **INVITED**

Since the establishment of techniques for surface conductivity measurement by microscopic four-point probes (M4PP).[1-5] with four-tip scanning tunneling microscope (4T-STM) and monolithic four-point probes, electronic transport through single-atomic layers on semiconductor crystals has attracted considerable interests. The electrical conduction through atomic chains and nanowires can also be measured by the methods. Interesting transport properties of such atomic-scale structures have been revealed; the instability and atomic-scale defects intrinsic to such nano-scale structures play decisive roles in transport. I will introduce and summarize the following several topics in the talk. Recent advancements with metal-coated carbon nanotube tips in 4T-STM are also introduced.[11]) (1) A metal-insulator transition and strong anisotropy in conductivity of Indium atomic wire arrays.[1,6] (2) Resistance caused by monatomic steps on surface .[12] (3) Non-metallic conduction of metallic Au wires and monolayers[7,10] (4) Conductance of individual silicide nano-wires and carbon nanotubes.[8,9,13]

[1]T. Kanagawa, et al., Phys. Rev. Lett. 91, 036805 (2003).
[2]T. Tanikawa, et al., e-J. Surf. Sci. Nanotech. 1, 50 (2003)[http://dx.doi.org/10.1380/ejssnt.2003.50]
[3]S. Hasegawa, et al., J. Phys.: Condens. Matter 14, 8379 (2002).
[4]S. Hasegawa, et al., Surf. Rev. Lett. 10, 963 (2002).
[5]R. Hobara, et al., Rev. Sci. Inst. 78, 053705 (2007).
[6]T. Tanikawa, et al., Phys. Rev. Lett. 93, 016801 (2004).
[7]H. Okino, et al., Phys. Rev. B 70, 113404 (2004).
[8]H. Okino, et al., Appl. Phys. Lett., submitted.
[9]R. Hobara, et al., Jpn. J. Appl. Phys. 43, L1081 (2004).
[10]S. Yamazaki, et al., submitted to Phys. Rev. Lett.
[11]Y. Murata, et al., Jpn. J. Appl. Phys. 44, 5336 (2005); S. Yosimodo, et al., ibid. 44, L1563 (2005).
[12]I. Matsuda, et al., Phys. Rev. Lett. 93, 236801 (2004).
[13]S. Yoshimoto, et al., Nano Letters 7, 956 (2007).

2:40pm **NS+MS-TuA4 A Novel Approach for Electronic Nanotechnology of Carbon Nanotubes**, ***K.E. Hurst***, National Institute of Standards and Technology, *R.K. Ahrenkiel,* National Renewable Energy Laboratory, *T. Campbell,* ADA Technologies, *J.H. Lehman*, National Institute of Standards and Technology

We present a new measurement technique for measuring the recombination lifetimes of carbon nanotubes called the resonant-coupled photoconductive decay (RCPCD) method.[1] The carrier recombination lifetime is a fundamental property of carbon nanotubes which is typically determined by contact-based techniques or spectroscopic methods which do not readily allow characterization of bulk material properties. The measurement is based on a pump-probe technique in which an optical pump and a low frequency microwave probe are employed. RCPCD offers the first rapid, non-contact technique for routine nanometrology of carbon nanotube electronic properties. We demonstrate measurements of carrier lifetimes for multi-walled carbon nanotube and single-walled carbon nanotube thin films, where the ~30 μm thick films are deposited on a glass slide by an air-brush technique. We also consider the influence of material purity on the measurement of lifetimes in these nano-scale systems. Raman spectroscopy and UV-VIS absorption measurements provide further identification and characterization of nanotube samples to enable correlation of nanotube properties with the efficiency of charge transport in these samples. RCPCD is shown to be a fast and effective method for measuring the lifetimes of bulk carbon nanotubes, thereby overcoming present issues of routine carbon nanotube electronic nanometrology.

[1]R.K. Ahrenkiel, S.W. Johnston Mater. Sci. Eng. B 102 (2003) 161

3:00pm **NS+MS-TuA5 Properties of the Surface and Core Region of Single CdS Nanowires**, ***S.F. Alvarado***, IBM Research, Zurich Research Laboratory, Switzerland, *O. Hayden*, Siemens AG, Germany

The properties of the surface and core region of single CdS nanowires are characterized by STM-based cathodoluminescence under ultrahigh-vacuum conditions at room temperature. The CdS nanowires were fabricated using pulsed laser deposition via metal-cluster-catalyzed growth. A diluted nanowire suspension was used to flow-align the nanowires on a p-type Si substrate using microfluidic channels. Cathodoluminescence is excited by using the tip of an STM as a source of low-energy electrons ($100 < E_{kin} < 1000$ eV) at currents in the pico- to microampere range. The penetration depth of the incident electrons is approx. 1 nm at 100 eV and increases with kinetic energy up to a few nanometers at 1 keV. Therefore this technique allows one to probe the surface region of single nanostructures. A typical spectrum collected on a single nanowire exhibits a relatively sharp emission line centered at approx. 510 nm, with a full width at half maximum of 20 nm, and a much broader band centered at 750 nm. The intensity ratio of the 510 nm to the 750 nm line increases with increasing electron energy, indicating that the 750-nm emission arises from the surface regions of the nanowires, whereas the 510 nm line originates mainly from their core regions. In addition, cathodoluminescence images of single CdS nanowires, collected at different wavelengths, exhibit regions of enhanced emission as well as local variations of the ratio of surface and core contributions. A comparison of cathodoluminescence spectra collected on nanowires, on a CdS nanosheet, and on other structures, suggests a relationship between the ratio of surface-to-core emission and the quality of the nanowires.

4:00pm **NS+MS-TuA8 Helium-ion Microscopy for Nanostructure Characterization**, ***N.P. Economou***, *B. Ward, J. Notte, R. Hill, L.A. Stern*, Carl Zeiss SMT **INVITED**

We have developed the first practical He ion microscope, based on a unique gas field ion source. The source has highly desirable performance characteristics for building scanning ion microscopes with sub-nanometer probe sizes. A unique construction allows the source to provide stable output over useful lifetimes of several hundred hours, thus enabling the development of practical systems for microscopy and nanostructure characterization. An important aspect of the He ion microscope is the interaction of He ions with the sample being observed. As compared with electrons interacting with the same sample, He ions penetrate less deeply, scatter less and produce higher yields of secondary electrons; back-scattered ions are also present. Images produced with a He ion beam exhibit greater material contrast, higher resolution due to reduced interaction volume, and better signal-to-noise ratio. These factors combine to produce He ion images that often contain more and better information than electron images. Because of these inherent advantages, we believe the He ion microscope will become an important tool for the study of nanostructures. We will discuss the unique characteristics of the source, and present images produced from the microscope that demonstrate its advantages over currently available instruments.

4:40pm **NS+MS-TuA10 Study of Characteristic Fragmentation of Nano Carbon by the Scanning Atom Probe**, ***O. Nishikawa***, *M. Taniguchi*, Kanazawa Institute of Technology, Japan, *Y. Saito,* Nagoya University, Japan, *M. Ushirozawa*, Japan Broadcasting Corporation

Since the characteristic fragmentation of a material is closely related with the binding state between the atoms forming the material, multiwall carbon nanotubes (MWCNT), graphite nanofibers (GNF) and ultrapure graphite are studied by field evaporating these specimens and by mass analyzing the fragmented cluster ions with the scanning atom probe. Two kinds of MWCNT were analyzed: commercially available and laboratory fabricated MWCNTs. GNF is grown on a 304 stainless steel tip by thermal CVD. Purity of the analyzed graphite is 99.9999%. The mass spectra of both MWCNTs are quite similar, particularly mass to charge ratio M/n from 0 to 100. However, the commercial MWCNT exhibits many unidentifiable small

mass peaks throughout the mass range up to a few thousands. The most significant feature is the large mass peak at M/n = 340 which could be $C_{28}H_4$. The proposed structure of this cluster is a squarely arranged 8 hexagonal rings. This structure is suitable to form a tube. The mass spectrum of GNF is quite different from that of MWCNT and shows the highest mass peak at M/n = 278, $C_{23}H_2$. The proposed structure of this cluster is the triangularly arranged six hexagonal cells. Two corner carbon atoms of the triangle are hydrogen-terminated and third corner carbon atom is bound with an extra carbon atom. Two dimensional extension of the fragments shows a hexagonal ring formed by 6 hydrogen atoms terminating the carbon bonds and 6 extra carbon atoms forming a hexagon. The hydrogen hexagonal ring is quite similar to that of a kekulene molecule. The graphite exhibits two completely different mass spectra. One is quite similar to that of MWCNT showing the characteristic large mass peaks. The other closely resembles those of silicon and diamond. The number of detected ions decreases with mass. Thus, the largest mass peak is C^{2+} and then C^+. The clusters formed by the odd number of carbon atoms are more abundant than those of even number. Most clusters are doubly charged. This implies that the binding between carbon atoms in this analyzed section is strong and uniform and that the graphite has two phases: diamond and graphite. Although only few H^+ ions are detected from MWCNTs and GNF, most fragments contain more than 1 hydrogen atom. On the other hand few ions detected from the diamond-like graphite are bound with hydrogen.

5:00pm **NS+MS-TuA11 Nano-scale Surface Effects of Field Electron Emission from Zirconium and Hafnium Carbide**, ***W.A. Mackie,*** *G.M. Magera, K.J. Kagarice*, Applied Physics Technologies

An electron source for a high resolution SEM/TEM application should produce a high brightness, have a minimal energy distribution, and should be highly stable. In an application in which the resolution is limited by chromatic aberrations, one can improve the performance over a commonly used thermal field emission source, such as a ZrOW Schottky emitter, by using a cold field emission source (CFE). In CFE, the emitting area of the usable beam is small and understanding surface chemistry and effects are crucial to controlling emission stability. Single crystalline transition metal carbides have electron emission properties making them attractive candidates for CFE applications. We are reporting on field emission from (310) oriented single crystal ZrC and HfC. ZrC(310) has a relatively low work function axial emitting surface (3.4 eV) that has a low evaporation rate, is resistant to ion bombardment and sputtering, has a high melting point (~3800 K), and a very low surface mobility. The robustness of this material allows for repeated cleaning via high temperature flashing without changing the geometry of the emitting end form. These crystals are electrochemically etched and mounted in a mini Vogel mount to enable flash cleaning. Experimental I(V) data were taken from which angular intensity and reduced brightness were calculated. Experimental I(t) data were then taken and analyzed for current stability in both long term drift and short term noise. Results are highlighted from a 160 nm ZrC (310) operating at 0.02 mA/sr. Noise spectra were analyzed by FFT and found to be consistent with step and spike like noise associated with foreign atom migration and ion bombardment. Emission from small areas comprising <100 atom sites are dominated by the mobility of foreign atoms from ion back streaming and surface diffusion both arising from the high electric field. Using an annular area surrounding the beam emission area as a current monitor we were able to control fluctuations in the beam. This control ability results from the overlapping currents from both areas. Data are presented which demonstrate improved stability over a variety of vacuum conditions.

Manufacturing Science and Technology

Room: 615 - Session MS-ThM

Metrology and Characterization for Manufacturing

Moderator: J. Randall, Zyvex Corporation

8:00am **MS-ThM1 Measurement of GST Thin Film Composition and Thickness**, ***M. Ye***, *C.C. Wang, G. Conti*, Applied Materials, Inc.

Recent studies demonstrated that phase change memory (PCM) can achieve fast switching speed, good reversibility and scalability, making it the most promising alternative non-volatile memory (NVM) technology for the next decade. Currently PCM is being actively studied in semiconductor industry, with $Ge_2Sb_2Te_5$ (GST) being the most widely investigated material. GST film thickness and composition are two important quantities that require close monitoring in manufacturing. We have experimented with a number of measurement techniques including x-ray reflectivity (XRR), ellipsometry, wavelength dispersive x-ray fluorescence (WDXRF), energy dispersive x-ray fluorescence (EDXRF), energy dispersive spectroscopy (EDS), Rutherford backscattering spectrometry (RBS), x-ray photoelectron spectroscopy (XPS), inductively coupled plasma optical emission spectroscopy (ICP-OES), and low energy x-ray emission spectroscopy (LEXES). The advantages and limitations of the various characterization and metrology techniques for GST film composition and thickness measurement are compared. XRR can measure GST film physical thickness and density independently with good precision. Our study of WDXRF shows that there is little interference between antimony and tellurium peaks, and that GST film thickness and composition can be measured simultaneously with good precision. XRR and WDXRF can often provide complementary information, which can be very helpful for troubleshooting process and hardware issues. More details will be presented in the paper. In EDXRF and EDS measurements, antimony and tellurium peaks overlap, and good peak modeling is required to deconvolute the peaks to ensure accurate measurement. RBS in general is a very good standardless analytical technique. However its use for GST application is limited since it can not resolve antimony and tellurium peaks. Particle-induced x-ray emission (PIXE) can be used together with RBS at the cost of measurement accuracy, yet PIXE still requires peak profile modeling. ICP-OES provides reasonable accurate results, but it is a destructive technique and thus not practical for process monitoring. We have also looked into XPS and LEXES for GST-related applications. The effects of sputtering process parameters such as pressure, temperature and wafer bias on GST film composition are discussed. The GST film composition variation through a sputtering target life is also monitored.

8:20am **MS-ThM2 Gate Oxide Process Control Optimization by XPS in a Semiconductor Fabrication Line**, ***A. Le Gouil***, *N. Cabuil, P. Dupeyrat,* STMicroelectronics, France, *B. Dickson, M. Kwan,* Revera, *D. Barge,* NXP, *O. Doclot,* STMicroelectronics, France, *J.C. Royer*, CEA/LETI-Minatec, France

The introduction of thinner films such as 15-20 Å SiON gate oxides makes in-line metrology challenges more complex. Nitrogen dose in the SiON film is strongly process deposition dependent and is one key parameter of advanced CMOS technologies. Therefore, optimized process control has to be implemented in-line to ensure process stability. Measurement techniques such as X-Ray Metrology have to move from offline characterization laboratories to fabrication lines and ultimately to in-line metrology. Among these techniques, X-ray Photoelectron Spectroscopy (XPS) is one of the best adapted metrology methods to ensure nitrogen dose monitoring of SiON gate oxides. Until recently, decoupled plasma nitridation (DPN) process monitoring has been performed on monitor wafers. However, measurements performed on monitor wafers may not fully represent actual electrical properties at the device level. Measurements on production lots allow inline detection of process excursions and provide real time feedback of process chambers' stability. Additional productivity improvements are reducing consumption of monitor wafers and their processing as well as data acquisition for correlations with device reliability parameters. The implementation in production of SiON gate monitoring on production lots implies to fully characterize the nitridation process on patterned wafers. This study is dedicated to a comparison between monitor and patterned wafers of DPN processes for 65nm node technology and below. Measurements are carried out in a next generation XPS tool with a 35µm spot size and pattern recognition capability that enable material metrology on product wafers. XPS measurements on patterned wafers are performed in specific test structures which dimensions are 50µm x 70µm using an Al Ka monochromatic X-ray source. A larger X-ray spot providing higher signal level is available for measurements on monitor wafers. First, gate oxides will be characterized for each process and tool measurement precisions will be shown. Second, nitrogen dose and thickness uniformity over the wafer will be compared and discussed. Third, different mappings protocols will be studied to identify the best compromise between throughput and an optimized mapping representative of process distribution. Finally, we will conclude with a selection of an optimized process control strategy of gate oxides.

8:40am **MS-ThM3 The Helium Ion Microscope and Applications for Semiconductor Manufacturing and Characterization**, ***J. Notte***, *N.P. Economou, B. Ward, R. Hill*, ALIS Corporation (Carl Zeiss SMT)**INVITED**

ALIS Corporation (a Carl Zeiss SMT company) has developed a helium ion microscope which provides high resolution images with strong contrast mechanisms. Although technically a focused ion beam (FIB) the microscope operates more like a scanning electron microscope (SEM) but with higher resolution and stronger contrast. The technology and its general capabilities are being presented in another session. This paper addresses some of the semiconductor manufacturing applications which are well suited to the helium ion microscope. Process development and process monitoring require high resolution imaging and contrast mechanisms that are sensitive to material differences. The helium ion microscope is well suited to these tasks. In particular, the secondary electron images can reveal fine details which contain topographic or material information. Grain formation is evident through well established channeling contrast mechanisms. Electrical properties can be revealed by virtue of the beam induced voltage contrast effects. Images can also be generated from the scattered helium ions, providing the ability to distinguish different materials based on their atomic number. This also has the advantage of giving a resolution which is superior to the presently used EDX analysis. Testing has been conducted to look for any effects of damage to semiconductor devices. In particular, a series of tests were conducted to examine any possible effect on the transistor turn on voltages, Vt, after various exposures to helium ions. Test results show no measurable shift. Higher dosages have been tested to look for other signs of damage. Additional manufacturing applications will be presented.

9:20am **MS-ThM5 Characterization of Electronic Materials with Atom Probe Tomography**, ***T. Kelly***, Imago Scientific Instruments **INVITED**

Atom probe tomography provides three-dimensional structural and compositional analysis of materials at the atomic scale. It has been applied increasing frequently in the past few years to materials characterization challenges in the semiconductor industry. Specimen preparation advances have made it routine now to extract and analyze materials from wafers and even finished components. Major developments in LEAP technology by Imago Scientific Instruments have led to greater facility for running specimens and greater detail in quantitative analysis. Important examples of analyses of CMOS semiconductor structures and devices, thin-film multilayer structures, and even organic nanostructures will be shown.

10:00am **MS-ThM7 Structural Fingerprinting of Nanocrystals on the Basis of High Resolution Transmission Electron Microscopy and Open-Access Databases**, ***P. Moeck***, Portland State University, *P. Fraundorf*, University of Missouri at St. Louis

It is well known that many nanocrystals can not be identified from their powder X-ray diffraction pattern as it is customary for micrometer sized crystals. When nanocrystals are involved, i.e. the kinematic scattering approximation is sufficiently well satisfied for fast electrons; a new strategy for lattice-fringe fingerprinting from Fourier transforms of high-resolution phase contrast transmission electron microscopy (HRTEM) images is feasible. This strategy relies on crystal structure information that is transferred to HRTEM images in the weak-phase object approximation. Such information is contained in (i) the projected reciprocal lattice geometry, (ii) the phase angle distribution (in the imaginary part of the Fourier transform of HRTEM images), and (iii) the relative intensities at the positions of reciprocal lattice points. Systematic intensities close to zero at certain lattice points may suggest kinematical absences of diffracted beams, aiding the structural fingerprinting. Nanocrystal structure specific limitations to the application of this strategy are discussed. The first tests of this strategy have been promising and the whole procedure could be automated in the current generation of computer controlled HRTEMs. When automated, mixtures of nanocrystals could be analyzed both qualitatively and quantitatively. Since each nanocrystal would be identified individually and thousands of nanocrystals could be processed

automatically, the detection limits of lattice fringe fingerprinting could readily be pushed to levels that are by far superior to those of traditional powder X-ray diffraction fingerprinting. The Crystallography Open Database (COD, http://crystallography.net) and its mainly inorganic subset (http://nanocrystallography.research.pdx.edu/CIF-searchable/cod.php) are discussed because the whole lattice-fringe fingerprinting concept is only viable if there are comprehensive databases to support the identification of unknown nanocrystals. While the COD contains the atomic coordinates, space group, lattice parameters, and other crystallographic information for more than 50,000 compounds, we provide at the research servers of Portland State University in addition interactive 3D structure visualizations and theoretical 2D lattice-fringe fingerprint plots for approximately 10,000 compounds for the mainly inorganic subset of the COD.

10:20am **MS-ThM8 The CD-AFM Technique as a Mean to Accelerate Advanced Process Development for the 45nm Node and Beyond**, ***J. Foucher***, CEA-LETI-MINATEC, France, *E. Pargon,* LTM-CNRS, France, *P. Faurie,* CEA-LETI-MINATEC, France, *M. Martin*, LTM-CNRS, France

As devices dimensions and architectures move towards the 32nm node, CD metrology needs for both production process monitoring and process development must cope with new challenges affected by unknown new materials, architectures and processes. One of the main challenges for advance node requirement is the accuracy in CD metrology which becomes mandatory not only at the R&D level but also at the manufacturing level. By simplicity and also because there was no impact on production yield, the semiconductor industry has traditionally followed a single CD value for use in statistical process control as a representation of their products on a wafer. For advanced processes, the control of profile shape and Line Width Roughness (LWR) is increasingly critical and subsequently the need in metrology accuracy for improvement of sidewall angle (SWA) and LWR is necessary. Through various examples of process development as regards advanced lithography, front-end or back-end etching, we will show that the CD-AFM technique represents a great opportunity to add accuracy in the Semiconductor manufacturing world and will allow other metrology techniques to progress in term of accuracy and subsequently will permit to decrease R&D and manufacturing cost.

10:40am **MS-ThM9 Analysis of Ion Implantation Damage in Silicon Wafers**, ***R.K. Ahrenkiel***, University of Denver

Ion implantation has become the standard method for building high-density, microelectronic devices. Rapid thermal annealing (RTA) is required to activate the implanted donor and acceptor species. Also, RTA is required to heal the lattice damage created by heavy ion implants such as boron, BF2, phosphorous and arsenic. The RTA process is required to maintain the structural integrity of the semiconductor used for submicron-integrated circuits, as dopant diffusion will destroy the implantation pattern using a long-duration heat treatment. There is a trade-off between the maintenance of the implantation pattern and the elimination of radiation damage. A quick, efficient, and contactless diagnostic of the implantation damage is highly desirable in both research and production environments. The resonant-coupled photoconductive decay (RCPCD) technique uses a deeply penetrating, low-microwave-frequency probe in conjunction with pulses from a tunable laser source. The recombination lifetime of the implanted region decreases many orders of magnitude as a result of implantation. The implanted region has electrical transport characteristics that are similar to those of amorphous silicon. For example, the recombination lifetime of the implanted regions becomes sub nanosecond, and similar to that of amorphous silicon. I have found the doubled YAG laser frequency of 532 nm to be especially useful for sensitivity to implantation damage. RTA restores the crystalline structure, and the degree of restoration depends on the RTA process. The implantation damage is manifested in a sharp decrease in the recombination lifetime when using strongly absorbed light, that is primarily absorbed in the implanted region. In addition, the as-implanted layer acts as a "sink" for minority carriers that are generated in the undamaged crystalline regions. The lifetime increases with various annealing processes, and one can correlate the lifetime changes with the specific annealing protocol. I will also show data for the sheet resistance, which is correlated with the increase of lifetime in the implanted volume. In summary, I will present a method for quickly evaluating the damage elimination of various implantation-annealing processes.

Manufacturing Science and Technology

Room: 615 - Session MS-ThA

MEMS Manufacturing

Moderator: R. Ghodssi, University of Maryland

2:20pm **MS-ThA2 Double-Exposure Gray-Scale Technology for Improved Vertical Resolution of 3D Photoresist Structures**, ***L.A. Mosher***, University of Maryland, *B.C. Morgan*, U.S. Army Research Laboratory, *R. Ghodssi*, University of Maryland

We report the development of a new double-exposure gray-scale photolithography technique to batch fabricate three-dimensional structures in photoresist with improved vertical resolution. Deep reactive ion etching is used to transfer the patterned photoresist into silicon, enabling a complete three-dimensional microfabrication platform with many applications for MEMS devices, such as lenses and microengines. Gray-scale photolithography utilizes a photomask to spatially control the ultraviolet light intensity incident on a photoresist layer. This control is achieved by diffraction through sub-resolution pixels on the mask using projection photolithography. Projection optics keep only the zeroth order intensity, preventing the higher-order diffractions from reaching the wafer. The local pixel size is correlated to the transmitted intensity and therefore determines the height in photoresist after development. Vertical resolution, determined by the number of available pixels, is limited by the mask vendor. Current mask fabrication techniques allow for tens of pixel sizes, which is insufficient for some MEMS applications. We introduce a double-exposure gray-scale technique, utilizing two gray-scale exposures prior to a single development. In this technique, two pixel sizes are used with two partial exposures, resulting in a third unique photoresist height after development. By using all pixel combinations, we achieved an exponential increase in the number of available levels. Our initial test design utilized only eight pixel sizes, but realized 64 unique height levels in photoresist after development. We created an empirical model to correlate the pixel combination and exposure times with the photoresist height, which facilitates the design of pixel layouts for nearly arbitrary geometries. This model was used to optimize the exposure times to minimize the average and maximum vertical step height. We fabricated a seventeen-pixel test structure based on this model and observed a significant improvement over single-exposure. A decrease in the average vertical step height from 0.19 µm to 0.03 µm was achieved as well as a decrease in the maximum vertical step height from 0.63 µm to 0.24 µm. Detailed modeling parameters and experimental results from double-exposure gray-scale structures will be presented.

2:40pm **MS-ThA3 MEMS Manufacturing in a High Volume CMOS Wafer Fabrication Facility**, ***G.D. Winterton***, Texas Instruments Inc. **INVITED**

The original concept of the digital micromirror device (DMD) is a far cry from the current embodiment of today's devices. Design, process, and packaging innovations of the past decade have enabled Texas Instruments Digital Light Processing (DLP) devices capable of transitioning from on to off over 5000 times a second with native contrast ratios in excess of 4000:1. TI's philosophy is to manufacture the DLP MEMS device in an existing high volume CMOS wafer fab. This philosophy constrains the MEMS processes to be compatible with existing CMOS processes. Sharing the facility with standard CMOS allows TI to benefit from the economies of scale which exist in a high volume CMOS fab. The MEMS group has a dedicated team of development, integration, and process engineers embedded within the larger fab engineering organization. This facilitates synergy between the engineering teams and leverages the experiences of the larger organization. MEMS manufacturing has additional requirements not found on standard CMOS. Most MEMS are 3D devices requiring very tight control of film thicknesses to control the spacing between MEMS elements. Film stresses are of much greater concern in MEMS processing which has required additional control methodologies to be put in place to facilitate much tighter control than standard CMOS. TI DLP products utilize sacrificial photoresist layers to create the spacings between the MEMS elements. Standard lithographic tools and techniques are used to create the patterns and traditional plasma etching are used to define these features. The metal deposition process cannot use traditional sputter etch techniques due to the presence of photoresist on which the metal is being deposited onto. The metal must also be deposited at low temperatures to avoid resist reticulation. Photoresist stripping and cleaning techniques had to be developed which could integrate into the fab without affecting the sacrificial resist layers or inducing unwanted topography. Special care is paid to surface conditions to avoid stiction effects since metal-to-metal elements cone in direct contact during device operation. The final step prior to packaging is the plasma removal of the sacrificial resist layers to release the MEMS elements. Significant engineering effort has been dedicated to packaging since particles are a major source of defects. Control of the internal package environment is an area of special concern to control stiction during the lifetime of the product.

3:40pm **MS-ThA6 Manufacturing Challenges and Method of Fabrication of On-Chip Capacitive Digital Isolators**, ***P. Mahalingam***, *D. Guiling, S. Lee, R. Figueroa, W. Tian, Y. Patton, I. Khan*, Texas Instruments

Digital isolators permit high-speed data transmission in industrial and process control applications which involve hazardous voltage environments. Texas Instruments introduced on-chip capacitive isolation technology for digital isolated couplers which enables products to provide isolation voltage up to 7000Vrms and ~12000V surge capability. An innovative, robust method of manufacturing low noise, 10kV peak on-chip capacitive digital isolator integrated in a BiCMOS process flow is presented this paper. Silicon based on-chip capacitive isolators used here are fabricated in a high performance precision analog 5V, 0.3um digital CMOS process with extremely low noise performance, and uses a lightly doped bulk, p-type substrate. Electrical measurements of on-chip capacitors reported here follow UL 1577, IEC 60747-5-2, and CSA standards. These include two tests (a) ramped voltage test from 4kVrms to 10kVrms to force device breakdown, which would quantify highest allowable overvoltage (VIOTM) , and (b) pulsed constant voltage test where 50 short pulses of 8kV and higher (to force breakdown) at 1us intervals are applied to device under test (DUT) for both polarities of the device, bottom-injection and top-injection. In this work, on-chip capacitors used for high voltage isolation is built using a dielectric stack which is a combination of pre-metal oxide, and/or the various dielectrics from metal-1 to top-metal depending on whether the bottom electrode is moat or metal-1. The choice of dielectric employed in these capacitors is based on the results of a I-V measurement study which examined electrical breakdown voltage of various dielectric materials such as silicon nitride, silicon oxynitride, oxides such as HDP, TEOS at various film stresses. Silicon nitride and oxynitride have the best isolation properties and offer unique advantages in meeting the isolation capacitor requirements. The challenges of integrating silicon nitride and oxynitride films as part of a dielectric stack in CMOS metallization scheme, the influence of the order in which these films are deposited in the dielectric stack on isolation capacitor's BVrms capability, pulse voltage performance, and device reliability are discussed. A model is developed to optimize dielectric film stresses in order to ensure isolation capacitor manufacturability by allowing wafer warpage to be maintained lower than the regime in which stepper chucking errors occur during downstream lithography processes.

4:00pm **MS-ThA7 A Novel Crystallized Silicon Thin Film Transistor Based Piezoresistive Cantilever Label Free Biosensor**, ***C. Zhan***, *P. Schuele, J. Conley, J. Hartzell*, Sharp Laboratories of America, INC.

This paper reports a novel integrated biosensor based on the piezoresistive effect of laser crystallized silicon (c-Si) thin film. The sensor is comprised of a c-Si resistor integrated on a PECVD SiO2 cantilever using low temperature surface micromachining techniques. Once the cantilever is deflected mechanically, the electrical response of the integrated thin film resistor changes accordingly. The fabrication and measurement results of crystallized silicon thin film resistor on a cantilever are presented. Our unique laser crystallized a-Si film enables a high quality thin film piezoresistor be accommodated on a small and thin cantilever using MEMS surface micromachining techniques. The integrated piezoresistive cantilever transducer can be selectively functionalized and implemented in large arrays for biosensing applications. The device consists of a c-Si thin film resistor embedded in a PECVD SiO2 cantilever. The air gap between the cantilever and the substrate is defined by a PECVD a-Si sacrificial film, which was removed during release etch step. When the cantilever is deflected by an external force, pressure or surface stress, a uniaxial strain is induced along the longitudinal direction of the cantilever. The strain stretches or compresses the thin film resistor and therefore changes the resistance. The fabrication process is a standard TFT process flow compatible surface micromachining process. Only two extra masks, one for sacrificial mesa patterning and another for cantilever outline patterning, are introduced to the standard TFT flow to realize the c-Si TFT based piezoresistive cantilever biosensor. A 1.5 um thick a-Si is PECVD deposited as the sacrificial film and a TMAH based release etchant is used to release the MEMS cantilever. The PECVD SiO2 films of the standard TFT process are used to form the body of the cantilever. One design of the

cantilever is 140um long, 50um wide and 0.5um thick. The c-Si TFT active thin film is used to form the piezoresistor. The thickness of the active c-Si piezoresistor is 100nm. Initial tests on our fabricated MEMS piezoresistive biosensors confirm the piezoresistive effect. External mechanical actuation tests were performed using a micropositioner for calibration. The minimum detectable cantilever deflection is 3nm at 3dB signal to noise ratio. Currently, the sensitivity of the fabricated cantilever biosensor is 3.07uv/nm. The biosensing tests are on the way and results will be updated.

4:20pm **MS-ThA8 Divergence in N/MEMS and Semiconductor Manufacturing**, ***J.D. Evans***, Defense Advanced Research Projects Agency (DARPA) **INVITED**

Nano and Micro Electro-mechanical System (N/MEMS) technology seeks to build small devices (nano/milli scale features) using processing equipment similar to that utilized in the semiconductor industry. Because of similarities in scale and equipment, the performance and potential growth of N/MEMS, as an industry, has been often compared to the growth of the semiconductor industry. However, similarity of length scale and fabrication equipment is not sufficient to ensure similar market performance. In fact, the MEMS and semiconductor industry face dramatically different technical and market dynamics that cause one to question whether this comparison can allow one to draw any meaningful conclusions. In this talk, the author will focus on four fundamental differences between N/MEMS and semiconductor industries: (1) difference in scalability (with implications for a "Moores' Law for MEMS"), (2) difference in process diversity, (3) difference in manufacturing volume, and (4) differences in required fabrication precision (N/MEMS requires higher fabrication precision than semiconductors). These differences suggest that N/MEMS industry faces a fundamentally different set of technical and market constraints than faced by semiconductor industry, and lead one to expect a fundamentally different market evolution. While they do not diminish the fundamental importance of N/MEMS technology, the differences do suggest a need for N/MEMS specific expertise in evaluating and exploiting N/MEMS opportunities, and may suggest a need for a new set of fabrication technologies specifically designed for the N/MEMS markets. DARPA Distribution Statement "A": Approved for Public Release, Distribution Unlimited.

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