Tuesday Morning, October 16, 2007

Plasma Science and Technology

Room: 607 - Session PS2-TuM

Advanced Gate Etch

Moderator: T. Kropewnicki, Freescale Semiconductor

8:00am **PS2-TuM1 Reaction Mechanisms in Patterning Hafnium Aluminate High-k Thin Films**, ***R.M. Martin*****, University of California at Los Angeles, *H.-O. Blom,* Uppsala University, Sweden, *J.P. Chang*, University of California at Los Angeles

The development of plasma etching chemistries is necessary to pattern new gate dielectric materials, such as hafnium-based oxides, for sub-45nm CMOS devices. Hafnium aluminates ($Hf_{1-x}Al_xO_y$) have arisen as a promising material for gate oxide replacement due to their high dielectric constant, bandgap, and recrystallization temperature. Hafnium aluminates with the Al_2O_3 content varying from 0 to 100% were synthesized to study the effect of alumina addition to hafnia. An electron cyclotron resonance high density plasma reactor was used in this work to study the etching of hafnium aluminates in chlorine-based chemistries. The plasma density, electron temperature, and gas phase reactive species were characterized by a Langmuir probe, optical emission spectroscopy, and quadrupole mass spectrometry (QMS). $Hf_{1-x}Al_xO_y$ films were etched in Cl_2 and BCl_3 plasmas and the etch rate scaled linearly with the square root of ion energy at high ion energies (> 50 eV), however the etch rate in BCl_3 was 1.5 to 2 times that in Cl_2. The faster etch rate in BCl_3 was attributed to a change in the dominant ion from Cl_2^+ to BCl_2^+ as determined by QMS. At low ion energies, (< 50 eV), a physical-sputtering-like process was observed in Cl_2 while deposition was observed in BCl_3. The dominant metal-containing etch products were $HfCl_x$ and $AlCl_x$ in Cl_2 plasma and $HfCl_x$, $HfBOCl_4$, $AlCl_x$, and Al_2Cl_x in BCl_3 plasmas, and increased with ion energy. Oxygen was detected removed in the form of ClO in Cl_2 and $(BOCl)_3$ in BCl_3 plasmas. The etching threshold energy can be tuned by about 2 eV by changing the film composition, making it possible to design a composiiton near the interface to maximize the etching selectivity with respect to silicon. Chlorine was measured on the surface of all etched films (0-3 at. %) as well as boron (~7 at. %) for the BCl_3-etched films. The surface chlorination was enhanced with increasing ion energy, demonstrating that the etching reaction is limited by the momentum transfer from the ions to the film surface. Finally, a generalized phenomenological model will be presented to elucidate the effect of Al_2O_3 addition on modifying the etching characteristics of HfO_2.

8:20am **PS2-TuM2 Tungsten and Tungsten Nitride Etch Characterization for sub 45nm Metal Gate**, ***T. Morel,*** STMicroelectronics France, *S. Barnola,* CEA-LETI France, *O. Joubert*, CNRS/LTM France

Continuing downscaling of structures involved in advanced CMOS devices brings new complexity in plasma etching processes. The introduction of new materials, (metal gates, high-k dielectrics) to avoid the poly depletion effect and to minimize the equivalent oxide thickness, requires new dry etch approaches. Innovation proposed here is the use of thin MOCVD tungsten or tungsten nitride layers (10nm) to achieve PMOS devices on 300mm wafers. In this work, we characterized both metal layers by angle resolved X-ray Photoelectron Spectroscopy (XPS) and X-Ray Reflectometry (XRR). It is found that W and WN layer present differences in terms of oxygen and carbon concentration and density. To get a better understanding of interfaces between the different layers of a complete gate stack (Poly-Si / TiN / WN or W / high-k), Secondary Ion Mass Spectroscopy (SIMS) and XPS depth profiling were performed. The characterization of as-deposited and integrated tungsten alloy revealed variations between both metals that involved two different strategies to achieve good profile in patterned metal gate electrode. Concerning the process development, etch rates of W and WN were carried out in chlorine and fluorine based chemistries on a 300mm ICP tool with in-situ optical emission spectroscopy and in-situ interferometer. With the support of ion mass spectroscopy and quasi in-situ XPS, etch mechanisms of tungsten alloy were identified. Finally, the integration of W and WN etch into a multiple steps process for sub 45nm metal gates were investigated. Cl_2-O_2 and Cl_2-O_2 with additional fluorine are the proposed solutions to control, respectively, the profile of tungsten nitride and tungsten, without damaging the passivation on the Poly-Si sidewalls.

8:40am **PS2-TuM3 Nitride Spacers Dry Etching for sub-20nm HfO2 - Metal Gate on Fully Depleted SOI**, ***C. Arvet,*** STMicroelec., FR, *J. Chiaroni, V. Loup,* CEA-Léti/Minatec, FR, *P. Besson,* STMicroelec., FR, *P. Brianceau,* CEA-Léti/Minatec, FR, *M.P. Clement,* STMicroelec., FR, *V. Delaye, L. Tosti, C. Buj,* CEA-Léti/Minatec, FR, *O. Louveau,* STMicroelec., FR, *E. Vermande, M. Heitzmann, S. Barnola,* CEA-Léti/Minatec, FR, *R. Blanc*, STMicroelec., FR

Fully Depleted Silicon on Insulator is one of the most promising MOS transistors fabrication technologies to address low power and high speed applications challenges. Due to the very thin channel silicon thickness, selective epitaxial growth is mandatory to raise source and drain areas. So in addition to there classical uses as sidewall for ion implantation, spacers play a major role to avoid leakage current between metal gate and raised source and drain. On this way new constraints appear for nitride spacer dry etching. An accurate control of etch polymers is mandatory to allow a good performance of the next step, while a very high selectivity to thin silicon, silicon dioxide and HfO2 materials is required to avoid any silicon surface damage or HfO2 modification. Indeed, typical HfO2 thickness is less than 3 nm, thin silicon film is 10 nm or less while silicon dioxide hard mask on top of the gate must not be impacted. Moreover, two different approaches can be used for gate stack building. In the "spacer first approach", the nitride layer is deposited over the HfO2 material then spacers are etched, while in the "spacer last approach", the HfO2 is etched before nitride layer deposit. This affects the requirements for spacer etch, resulting in two different dry etch processes. These processes were developed in a DPS2 (Decoupled Plasma Source) Applied Material reactor either with a CH2F2 based chemistry or a CF4/HBr based chemistry. Etch rates, selectivities and non uniformities were optimized by adjusting gas ratio, source and bias RF power. SEM Cross sections, SEM-CD and TEM demonstrate good spacers profile and metal gate coverage. A 1.5 nm range spacer size control has also been reached, although spacer size adjustment by use of the overetch step seems to be limited. Plasma impact and selectivity to HfO2 and Silicon were measured by ellipsometry and XPS analysis. Results show no consumptions for HfO2 and less than 1.5 nm for silicon. A CFx polymer deposition allows high selectivities and no HfO2 modification. Post nitride dry etch XPS and particle measurement show also that HF wet chemistry is required to fully achieve High-K removal and optimize next integration steps. From these experiments, robust processes were developed. Electrical test of sub-20nm HfO2 and TiN Metal Gate on Fully Depleted SOI will be presented with the two integration schemes. This work has been carried out within the frame of Léti/Minatec-Crolles2 alliance program.

9:00am **PS2-TuM4 XPS Sidewall Analyses of Poly Si/TiN/HfO_2 Gate Stack Etched with Chlorine and Fluorocarbon Based Chemistries**, ***O. Luere***, Freescale Semiconductors, France, *L. Vallier, E. Pargon,* LTM-CNRS, France, *L. Thorsten*, Applied Materials

Patterning sub-40 nm metal gates on high k dielectrics is one of the biggest challenges for the fabrication of next generation devices. The metal gate etching step is, indeed, difficult: it must be highly anisotropic to maintain a tight CD control (≤ 2 nm) and must not damage the underlying high k material. In this work, we have investigated and compared the impact of the etching of the TiN layer in a Poly Si/TiN/HfO_2 gate stack using Cl_2/HBr and SF_6/CH_2F_2 based chemistries. The experimental work has been performed on a 200 mm etch platform connected, under vacuum, to an x-ray photoelectron spectroscopy surface analysis system. In order to better understand the etching mechanisms, we have used a technique based on X-ray photoelectron spectroscopy (XPS) to analyse the passivation layer deposited on the sidewalls of the patterns during the Polysilicon etching step and investigate its modification during the TiN etching step. We also used SEM pictures to analyse the gate profiles and determine the thickness of the passivation layer. The etching of polysilicon with a Cl_2/HBr based chemistry requires the introduction of O_2 in the plasma in order to form a SiOClBr layer which protects the polysilicon sidewalls. On the contrary, the etching of TiN must be O_2 free to prevent the metal oxidation. The absence of oxygen in the plasma gas phase during TiN etching can potentially lead to a modification of the passivation layer formed on the Polysilicon sidewalls. Nevertheless, We have shown that, using appropriate plasma conditions, the SiOClBr layer deposited on the chamber walls during Polysilicon etching is eroded during the TiN etch step, leading to an increase of the passivation layer thickness on the Polysilicon sidewalls. Same analyses using a SF_6/CH_2F_2 based chemistry will also be presented.

* PSTD Coburn-Winters Student Award Finalist

9:20am **PS2-TuM5 Reactive Ion Etching of Ru Compounds Modified by Ion Implant**, ***C. Park***, *B.S. Ju, S.C. Song, M. Cruz,* SEMATECH, *B.H. Lee, R. Jammy*, IBM

One of the technical hurdles for implementing high-k / metal gate in advanced CMOS is high threshold voltage (V_{th}) in p-MOSFETs. Recently, it was shown that the V_{th} of p-MOSFETs can be lowered by using Ru compounds as a metal gate on HfSiO high-k dielectric. Gate etch requires good local and global etch uniformity across the wafer without damaging the underlying gate dielectric. Unlike Ru or RuO_2 films, Ru compounds have high etch resistance with conventional etch chemistries, which imposes a significant technical challenge on gate stack patterning. It is possible to etch Ru compounds by applying higher than normal bias power. A high bias power etch, however, poses the high risk of forming either a micro-trench or footing on the pattern sidewall and causing a rough patterned sidewall as well as punch-through of the gate dielectric. It was demonstrated that ion implant could modify the bond structure of Ru compounds, so that they could be etched in a highly controlled manner with O_2/Cl_2 plasma. Optimum implant condition, which enables plasma etch of the Ru compounds, was found by splitting of implant energy and dose conditions. The effects of the ion implant on film thickness, bonding of Ru compounds, and knock-on of Ru compounds and gate dielectric into silicon substrate were also studied.

9:40am **PS2-TuM6 Plasma Etching Processes for Aggressively Scaled Gate Features**, ***N.C.M. Fuller***, *M.A. Guillorn, Y. Zhang, W.S. Graham, E.M. Sikorski*, IBM TJ Watson Research Center

Scaling of device dimensions for 32nm and beyond technology nodes demands process, integration and tooling innovations to meet feature profile, line edge roughness (LER) and line width roughness (LWR) requirements. To these ends multi masking schemes have been employed to attempt to enable scaled devices and reduce LER/LWR constraints. Further, we have utilized various process conditions to increase the mechanical integrity of patterning materials in such multi masking schemes patterned with mixed electron beam and optical lithography. This methodology has enabled 20nm gates on a 60nm pitch with 0.5-1.0nm improvement in post lithography LER/LWR and 100% physical yield. These and other results will be presented and discussed.

10:40am **PS2-TuM9 Investigation of 45nm Silicon Gate Etching Process Variability Contributors**, ***L. Babaud***, Freescale Semiconductor, France, *P. Gouraud,* STMicroelectronics, *O. Joubert, E. Pargon*, CNRS/LTM, France

In a semiconductor world more and more aggressive in term of device performance and market cost, the control of critical dimension for 45 nm poly gate and beyond appears as a big challenge. Indeed as conventional photolithography is not able to define the novel design targets, other strategies as the double patterning on complex stack are developed. But the introduction of such complex process will induce additional sources of dimension variability and so alter the final functionality of the device. In this way, the research of the variability contributors from lot to lot, wafer to wafer, site to site will be the keys of an understood and controlled process. Some new parameters such as Line Edge Roughness (LER) will have to be considered. This presentation will focus on profile and dimension variability studies of the different steps of a gate stack process integrating a Hard Mask. Moreover we will investigate the impact of the 300 mm industrial ICP chamber walls conditioning strategies on the gate morphology. Chemical topography analyses by X-Ray Photoelectron Spectroscopy (XPS) will be performed to correlate the morphological results with passivation layer composition, deposited during the silicon etch process.

11:00am **PS2-TuM10 Control of SiO_2/Si Interface States during Plasma Etching Processes**, ***Y. Ishikawa***, *Y. Ichihashi,* Tohoku University, Japan, *S. Yamasaki,* National Institute of Advanced Industrial Science and Technology, Japan, *S. Samukawa*, Tohoku University, Japan

Plasma processes are indispensable in the fabrication of MOS LSI devices. During plasma processes, however, serious problems can occur, such as charge-build up damage and UV photon irradiation damage. In particular, UV irradiation from the plasma causes drastic degradation of sub-50nm MOS LSI device characteristics, because the penetration depth of UV photons into dielectric films is more than 10nm. We have previously reported that UV photons from plasma effectively generate E' centers (Si dangling bond in SiO2 film) in SiO2 films. However, the relationship between UV irradiation from plasma and interface states' (Pb centers, Si dangling bond at SiO2/Si interface) densities must be basically understood during the plasma process, because the generation of interface states directly degrades the electronic properties of MOS LSI devices. We focus on SiO2/Si interface state density trends during conventional continuous wave (CW) plasma and pulse-time-modulated (TM) plasma etching processes. In order to evaluate the generation of interface state density, 5nm thick thermally grown SiO2 films were formed on Si substrates. The SiO2 films were then irradiated using Ar inductively coupled plasma. After that, we evaluated the Pb centers using electron spin resonance spectroscopy. Before the plasma irradiation, the density of the Pb centers was less than $1x10^{10}$ cm^{-2} spins. After the Ar CW plasma irradiation, and without any substrate RF bias power, Pb centers drastically increased. That is, the Pb centers increased drastically even after irradiation using conventional Ar CW plasma and elimination of ion bombardment. We also investigated the dependence of ion bombardment energy on the density of Pb centers in conventional CW plasma. However, even when 100W of RF power was applied during the plasma process, the ESR spectrum did not change. This result indicates that Pb centers are mainly generated by irradiation with UV photons during plasma processes. Therefore, we investigated the effects of TM plasma on eliminating Pb centers. During the TM plasma irradiation, the UV photon irradiation was drastically reduced during the plasma's "off" period. After the TM plasma irradiation, the Pb centers densities reduced dramatically to less than $1x10^{10}$ cm^{-2} spins, compared to those observed after CW plasma irradiation. We found that TM plasma was the most promising candidate for the elimination of Pb centers during the plasma etching processes.

11:20am **PS2-TuM11 Plasma Etching in the Era of Intensive Integration Innovation**, ***Th. Lill***, Applied Materials, Inc. **INVITED**

Driven by relentless pursuit of Moor's law, plasma etching advances at a rate never before seen in the history of this IC processing technology. New challenges are posed by several significant co-emerging trends: 1. Pattern fidelity requirements within wafer and lot reach sub nanometer, i.e. atomic resolution. 2. Plasma Etching is now an integral part of pattern generation (resist trim, double pattering, multilayer resist schemes). 3. Aspect ratios increase almost inverse proportional to the nominal line width for any given technology node reaching 100:1 for capacitor silicon etches and 40:1 for capacitor dielectric etches. 4. The number of potential new material candidates and their possible combinations in future stacks is exploding. At a first glance these challenges are well known and represent just another incremental tightening of known requirements. In this paper, we will show that these trends lead to three new paradigms in plasma etching: divergence of plasma etch applications, convergence the required process space to cover these applications and the need for precision chamber matching. We will discuss the consequences for plasma etch engineers and show examples for how Applied Materials Etch is responding to these new paradigms today to provide productive solutions for whatever device and integration engineers hold in store for the plasma etch community.

12:00pm **PS2-TuM13 The Effect of Oxygen Addition in a Chlorine Plasma during Shallow Trench Isolation Etch**, ***C.C. Hsu***, *J.P. Chang*, University of California at Los Angeles

Shallow trench isolation has been widely used to electrically isolate adjacent transistors. The mixtures of chlorine and oxygen have been one of the most commonly used chemistries for the shallow trench isolation etching process. In this work, an electron cyclotron resonance high density plasma is used to study the effect of oxygen addition in a chlorine plasma during the etching of silicon. To quantitatively assess the effect of oxygen addition, the plasma density and the electron temperature were characterized by using a Langmuir probe. The plasma species, including the etching by-products, were studied using the quadrupole mass spectrometry and the optical emission spectroscopy. The silicon etching rate was measured in-situ by using laser interferometry. Scanning electron microscopy was used to observe the topography change of the etched blanket films. The silicon etching rates were found to increase with the square root of the ion energy with a 9 eV threshold energy, suggesting the etching reaction is limited by the momentum transfer from the ions to the surface. With a relatively small amount of oxygen addition to the chlorine plasma, the etching rate remained approximately constant while the by-product identity and its distribution changed significantly. The dominant ionic etching by-products in chlorine plasmas were $SiCl^+$ and $SiCl_3^+$, but changed to $SiCl^+$, $SiOCl_2^+$, and $SiCl_3^+$ with the oxygen addition. The roughness of the etched surface increased significantly with oxygen addition. The significant changes of the by-products distribution and the etched surface topography suggest that the etching mechanism changes with the oxygen addition to the chlorine plasmas.

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