Plasma Science and Technology

Room: 607 - Session PS2+MS-MoM

Plasma Etching for Advanced Interconnects I

Moderator: V. Ku, Applied Materials

8:00am **PS2+MS-MoM1 Challenges for Microwave Plasma Etching of Low-k Dielectrics**, ***T. Nozawa***, *M. Inoue, T. Nishizuka*, Tokyo Electron LTD Japan **INVITED**

Meeting post 32 nm etch process integration requirements with porous SiCOH and conventional plasma sources is a challenge as the SiCOH surface is decomposed by reactions induced by electron, ion, radical and UV radiation exposure. This exposure is inherent to most plasma systems making it difficult to achieve both high precision and damage free etching. Neutral beam etching has been developed to provide ion and UV radiation free and therefore damage free etching processes. Neutral beam etching by itself lacks the benefits of energy and chemistry control afforded by in-situ plasma processes. A Radial Line Slot Antenna (RLSA) driven surface-wave-plasma at 2.45GHz generates very high density plasma with high electron temperature in a region limited to just below the dielectric plate through which microwave pass. Both chemistry and energy control are achieved with the RLSA configuration. Plasma is transported to the wafer by diffusive transport through a low electron temperature region. An electronegative precursor gas (e.g., C4F8) is injected into the low electron temperature region so that dissociation is not excessive and a substantial negative ion population is generated near the wafer. An RF bias frequency 400kHz through the wafer provides ion acceleration without plasma generation. The combination of the low electron temperature electronegative downstream plasma with the low driving frequency facilitates charge damage free etching for all process conditions. Another consequence of the combination of plasma conditions near the electrode is that physical damage of SiCOH material is eliminated and k-value increase is minimized. This is achieved through dissociation control which results in the population reduction of small very reactive species such as H* and F* and the retention of sidewall polymer integrity. The unique plasma characteristics of the RLSA system will be described in this presentation with an emphasis on process performance for post 32 nm node CMOS fabrication.

8:40am **PS2+MS-MoM3 High Frequency Capacitively Coupled Plasma for Low Ion Energy Dual Damascene Etching**, ***A. Marakhtanov***, *E.A. Hudson, K. Takeshita, O. Turmel*, Lam Research Corp.

Capacitively coupled discharges are widely used for semiconductor processing, especially in the area of dielectric etching. With a wide range of film materials and complex stacks including multiple mask layers, advanced dielectric etch processes require tight control of plasma parameters, such as ion flux, radical composition, and ion energy distribution (IED). This paper presents IED measurements and patterned-wafer etch results as a function of RF bias excitation frequency applied to the wafer electrode. The aim is to produce the optimal IED for etching of soft materials, such as low-k dielectrics commonly used in Dual Damascene interconnect schemes. One key challenge arises in the trench etch step, which requires a vertical etch profile in the low-k film. But the process must avoid corner faceting of any exposed via holes or of the hard mask layer which defines the initial trench pattern. Faceting would cause an increase in via or trench critical dimension, respectively. The competing requirements of vertical profile and minimal faceting define a fairly narrow range of acceptable ion energies for the process. If power is held constant, higher RF driving frequencies typically produce plasmas with higher densities and lower potentials, and enable operation at lower pressure. Both the mean ion energy and width of the IED reaching the wafer tend to decrease as the wafer bias frequency increases. For frequencies too low, the width of the IED is too large and faceting is induced by the high energy ions. For frequencies too high, the mean IED is too low to etch the low-k film with a vertical profile and acceptable rate. Results show that the necessary IED for these applications can be obtained by applying 60MHz to the wafer electrode.

9:00am **PS2+MS-MoM4 Energy Distribution of Bombarding Ions, Etch Selectivity and Profile Control in Plasma Etching of Dielectrics**, ***F.L. Buzzi***, *Y.-H. Ting, A.E. Wendt*, University of Wisconsin-Madison

The energy distribution of bombarding ions during plasma etching of dielectrics for microelectronics manufacturing affects both selectivity to photoresist and the profile shape of the etched feature. Here we examine the role of ion bombardment making use of an ability to produce either a narrow ion energy distribution (IED) at a specified energy, or a two-peaked distribution in which the energy and relative flux of the two peaks can be controlled. A system has been developed for manipulating the IED at the substrate during plasma etching by controlling the voltage bias waveform of the RF bias applied to the substrate. The output of a waveform generator drives a broadband power amplifier connected to the electrode, and is programmed in an iterative process to produce the desired substrate wave form. The iterative feedback process has recently been automated so that arbitrary waveforms can be quickly achieved. Waveforms to produce ions at the substrate with energies greater than 500 eV in single-peaked or two-peaked IEDs are now routinely produced, and are applied to etching of silicon dioxide in fluorocarbon-based gas mixtures. Prior studies with a single-peaked IED at energies below 200 eV showed significant improvements in etch selectivity compared to a sinusoidal bias producing a broad IEDF (Wang and Wendt, 2001, Silapunt et al., 2003). In this study, we will report on a systematic characterization of IED effects on blanket and patterned wafers. Results include the following: 1) effect of ion energy on photoresist and oxide etch rates for the narrow single-peaked IED at high energy, 2) effect of ion energy on photoresist roughening/distortion, to explore evidence of improved performance with higher energy ions, and 3) systematic study of the asymmetric bimodal IEDs as a function of the relative ion fluxes at the two energies, to examine the effect on etch rates for oxide and photoresist and etched feature profiles. The plasma system is equipped with a helicon plasma source operating at 13.56 MHz. The substrate electrode accommodates 4" diameter wafers, and is equipped with helium backside cooling and a thin film laser interferometer to monitor etch rates of blanket films. The chamber walls are heated externally to minimize process drift associated with wall temperature changes during plasma operation.

9:20am **PS2+MS-MoM5 Etch Plasma Chemistry and Film Variability Effects on Dual Damascene Patterning of Porous Ultra-low k Materials**, ***C.B. Labelle***, AMD, Inc., *J. Arnold,* IBM Research, *H. Wendt,* Infineon Tech., *R.P. Srivastava,* Chartered Semicon. Mfg Ltd., *K. Kumar, Y. Choi, H. Yusuff, S. Molis, C. Parks, C. Dziobkowski, M. Chace, A. Passano, L. Tai,* IBM Microelectronics, *D. Kioussis,* AMD, Inc., *J. Yamartino, D. Restaino, L. Nicholson*, IBM Microelectronics

Porous ultra low k dielectrics (k < 2.5) are being integrated into current and future technology nodes. A large focus of the integration of these films has been on the sensitivity of the films to compositional modification (i.e., carbon depletion) during resist strip in the dual damascene patterning scheme. As porous ultra low k dielectric strip processes have evolved and matured, new sensitivities have emerged which affect successful integration. This paper will discuss a case where, in a via-first-trench-last dual damascene integration scheme, the plasma chemistry used during via etch has been found to affect the profiles after trench etch when etching porous ultra low k dielectrics ("ULK via/trench interaction"). Modifications to the via etch plasma chemistry can be made to bring the trench profile back to target, but repeatability of the success of these workarounds is key. Variability in the film composition through the bulk of the film can also instigate post-etch profile changes or exacerbate the etch plasma-induced via/trench interaction. Data will be shown demonstrating the sensitivity of the etch processes to film composition variability. Possible mechanisms for the ULK via/trench interaction will also be discussed.

9:40am **PS2+MS-MoM6 Surface Roughening Mechanisms during Porous SiOCH Etching Processes**, *F. Bailly,* CNRS/IMN - France, ***T. David***, CEA/LETI-MINATEC - France, *T. Chevolleau, M. Darnon,* CNRS/LTM - France, *C. Cardinaud*, CNRS/IMN - France

Introducing dual damascene structures for the interconnections has been a means of improving their electrical performances. However, lowering the effective dielectric constant remains a major stake. Increase the porosity of the dielectric material or remove the trench bottom etch stop layer are some solutions. As a result, the trench etch process is stopped into the porous material which may lead to a tricky trench bottom roughness. In addition, sidewall metal diffusion barriers have to be thinned down to keep the copper line resistance low. In this context, the trench bottom roughness may also affect metal barrier coverage. In this study, roughness of dielectric materials is characterized by SEM and AFM after partial etching. Dielectric etching is known to be controlled by the thickness and composition of a fluorocarbon overlayer which depends on the plasma characteristics (etch chemistry…) and on the materials properties (composition, porosity,…). Thereby, in order to understand the mechanisms controlling the porous SiOCH roughening, different etch plasmas have been performed on materials with different percentages of porosity (7, 25 and 30%). For a high polymerizing (CF_4/Ar/CH_2F_2), a low polymerizing (CF_4/Ar) and a pure

physical sputtering plasma (Ar), surface composition has been characterized by quasi in situ XPS and the roughness has been studied as a function of the etched thickness. Those experiments highlight different trends. Firstly, the 7 % porous SiOCH does not exhibit any significant roughness whatever the etching plasma (rms roughness = 0.5nm). Secondly, porous SiOCH with a higher porosity (25 and 30%) is roughened when exposed to fluorocarbon based plasmas. The resulting roughness increases linearly versus the etched thickness in the range of a tenth of nanometers. This increase is fast when the concentration of fluorocarboned species at the etched surface is low, while a higher amount of fluorocarboned species limits it. At last, sputtering of porous SiOCH using a pure Ar plasma, namely the absence of fluorocarboned species at the etched surface, leads to a surface as smooth as the pristine material (rms roughness = 0.2 nm). Those results highlight the critical role of porosity and the presence of fluorocarboned species on the dielectric surface roughening. On the basis of those observations, a hypothesis will be proposed for the initiation and maintaining of the dielectric roughness.

10:20am **PS2+MS-MoM8 Design for Manufacturability through Design-Process Integration***, **A. Neureuther***, University of California, Berkeley **INVITED**

Exploratory prototype Design for Manufacturing (DFM) tools and methodologies are described. Examples will include new platforms for collaboration on process/device/circuits, visualization/quantification of manufacturing effects at the mask layout level, and fast/approximate physical modeling for first-cut design decisions. The examples have evolved from research supported over the last several years by DARPA, SRC, Industry and the U.C. Discovery Program on aberrations, illumination, polarization, CMP, plasma etching and device variation. DFM tools must enable complexity management with very fast approximate models across process, device and circuit performance with new modes of collaboration. Circuit Designers have good complexity management skills can add value by participating in this collaboration. Collaborations can be promoted by supporting multiple views of the trade-offs in terms of the natural intuitive parameters of each collaborator. Many of the nonidealities of manufacturing can be expressed at the mask plane in terms of lateral impact functions. This allows visualization and quantitative assessment of effects that are not easily captured even with large sets of design rules. Pattern Matching and Perturbation Formulation have promising exceptional speed and adequate accuracy for implementing these lateral impact assessments.

11:00am **PS2+MS-MoM10 Feature Profile Simulation for Organic Low-k Etching in 2f-CCP in H_2/N_2**, ***T.Y. Yagisawa***, *T. Makabe*, Keio University, Japan

As the size of ULSI continuously shrinks up to 45 nm in 2010 and multi-layer interconnect with more than 12 layers is applied, RC (resistance-capacitance) signal delay should be made smaller to meet the demand for higher performance of signal transmission. The dielectric constant of interlayer dielectric (ILD) can be reduced by lowering electric polarizability of the material. Alternatively introducing nano-holes within the material to reduce its density, decreases the k value. Increasing porosity is considered as a promising candidate for obtaining low-k ILD, though it may bring up new serious problems in its processing. Materials with low dielectric constant tend to possess poor mechanical strength and adhesiveness to the wire. In addition, low-k dielectric has low heat conductance and low resistance against heat, which makes it difficult to go through the post annealing in back-end processes. Currently, H_2/N_2 plasma is developed as the most suitable tool for the etching of organic low-k material. The etching profile is determined under the balance among isotropic etching by reactive H radical, physical sputtering by energetic ions and surface protection by the deposition of N radical. In order to attain the optimal profile, detailed understanding of these elements throughout the whole plasma etcher is strongly required. We have developed an integrated simulation consisting of the flux-velocity distribution of reactive species and the feature profile evolution of organic low-k etching in two frequency capacitively coupled plasma (2f-CCP) in the admixture of H_2/N_2.[1] In the present study, we will first estimate the density of reactive species, such as H, N and NH_x radicals, generated mainly via direct dissociation from parent gas molecules. Further, the effect of dissociation degree on the etching profile will be discussed as a function of the mixture ratio of feed gases.

[1]K. Ishihara et. al., Plasma Physics and Controlled Fusion, 48, B99 (2006).

11:20am **PS2+MS-MoM11 Removal of Scallops formed during Deep Via Etching for 3D Interconnects**, ***Y.-D. Lim***, *S.-H Lee, C.-H. Ra, W.J. Yoo*, Sunkyunkwan University, Korea

Three dimensional (3D) integration using chip-to-chip interconnects is currently receiving great attention since it can bring about substantial advantages in high packing density, low power consumption and high speed operation over planar circuits integration. Deep etching of high aspect ratio vias is known be the most critical step to realize the 3D interconnects. When the Bosch process which alternately introduces SF6 for isotropic etching and C4F8 for sidewall passivation is implemented to form deep via holes, the formation of scallops along the sidewall is unavoidable and poses a serious obstacle to scale down design rule in this scheme. In this work, we investigated methods to remove scallops using post O2 based plasma treatment assisted by subsequent HF based wet etching treatment, when inductively-coupled plasma etching had been applied to form various via hole sizes down to 2.5um with depths up to 100um. According to the experimental results, the removal of scallops was dependent on the via hole size, the orientation of scallop directed out of the sidewall, the combination of the post plasma etching chemistry and the subsequent wet etching chemistry, and the profile of etched structure. Furthermore, it was found that the removal of scallops is more effective for vias of larger and for more vertical structures. The technology developed in this work was proven to be suitable for subsequent electroplating of Cu interconnects.

11:40am **PS2+MS-MoM12 High-rate Deep Anisotropic Silicon Etching with the Expanding Thermal Plasma Technique**, ***M.C.M. van de Sanden***, *M.A. Blauw,* Eindhoven University of Technology, Netherlands, *F. Roozeboom,* NXP Semiconductors Research, *W.M.M. Kessels*, Eindhoven University of Technology, Netherlands

Emerging microsystem and 3D interconnect technologies require high anisotropic etch rates to accommodate Si etch depths exceeding 200-300 µm and aspect ratios higher than 10. Using inductively coupled plasma (ICP) reactors there has been a steady improvement of the performance of deep anisotropic Si etching, however, it is unclear whether sufficiently high etch rates can be obtained by continuous innovation of the existing ICP technology. Following our work on high-rate deposition of a wide variety of materials, we have explored deep anisotropic Si etching with the expanding thermal plasma (ETP) technique using fluorine-based chemistries. The ETP technique consists of a remote high-density plasma source and due to a low downstream electron temperature (< 0.3 eV) it has a good control of the plasma chemistry and ion energy. Both a cryogenic etching process and a time-multiplexed etching process were developed using SF_6-O_2 and SF_6-C_4F_8 etch chemistries, respectively. The ion energy was controlled by employing several substrate biasing schemes, including rf and pulse-shape biasing. In this contribution we will present data on etch rates, anisotropy, and selectivity with regard to the hard mask and it will be demonstrated that etch rates up to 12 µm/min and selectivities higher than 300 can be obtained by the ETP technique. Insight in feature profile control will also be presented and it will be shown that feature profiles are comparable to those obtained with ICP reactors. This novel, ETP-based deep anisotropic silicon etching technique might therefore be an attractive alternative for the fabrication of silicon microstructures with high-aspect-ratio features.

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