

Friday Morning, October 19, 2007

Nanometer-scale Science and Technology

Room: 616 - Session NS-FrM

Nanolithography and Nanoprocess Technology

Moderator: S. Pang, University of Michigan, L. Montelius, University of Lund, Sweden

8:00am **NS-FrM1 Stencil Lithography - Quick & Clean Surface Patterning at Mesoscopic Scales, J. Brugger, Swiss Federal Institute of Technology (EPFL), Switzerland** **INVITED**

Stencil lithography is a surface patterning technique that relies on the local physical vapor deposition of material through miniaturized shadow mask membranes. It is extremely useful for the formation of patterns, mainly thin structured metal films, in situations where lithography equipment is not available or when the surfaces don't allow the chemical and thermal process steps typically involved in photolithography. Stencil lithography is scalable from mm to sub-100-nm sizes, which makes it very interesting as method for rapid-prototyping of nanostructures without the risk of contamination, and for laboratories without access to high-end nanolithography equipment. The major challenges in stencil lithography are following: i) low-cost fabrication of nanostencils, ii) optimized mechanical properties of thin membranes, iii) deposition of material on stencil membrane, iv) precise alignment of nanostencils, v) recycling of stencils. In collaboration with our project partners¹ we have recently progressed in several of the above mentioned challenges. Stencils fabrication can be based on a set of advanced silicon micro and nanomachining steps (including UV, DUV, EBL and FIB) and a combination of DRIE and wet etching. The mechanical stability of the ultra-thin low-stress silicon nitride membranes could be considerably improved by topographic reinforcement rims. Surface structures of metals (e.g. Al, Au, Bi, Cr, Ti, Cu) on various surfaces (e.g. Si, SiO₂, SU-8, PDMS, PMMA, SAMS, freestanding SiN cantilevers, and curved surfaces) where systematically studied in terms of patterning accuracy. Thousands of sub-micrometer NEMS resonators were integrated in CMOS by stencil lithography and sacrificial etching. Variants of stencil methods include the local doping with ions, and local polymer etching using oxygen plasma. The talk will present the current state-of-the-art of nanostencil lithography, will highlight the strength of the method but will also discuss the current limits and challenges ahead to make it a truly reliable and scalable full-wafer nanofabrication method.

¹Integrated Project 'NAPA' European Commission and Swiss Federal Office OFES (Contract no. NMP3-CT-2003-500120).

8:40am **NS-FrM3 Nanopatterning of Functional Polymers by Thermal Dip-Pen Nanolithography, W.K. Lee, P.E. Sheehan, U.S. Naval Research Laboratory, W.P. King, University of Illinois, Urbana-Champaign, L.J. Whitman, U.S. Naval Research Laboratory**

Thermal dip-pen nanolithography (tDPN) uses a heated atomic force microscope (AFM) cantilever to deposit material that is solid at room temperature. The cantilever melts the solid ink on the tip, allowing precise control over its deposition onto the surface.¹ This method for nanolithography has proven particularly effective for depositing polymers.² Both the polymer thickness and lateral dimensions can be controlled to nanometer tolerances by controlling the tip heating power and the writing speed. Using tDPN, controlled layer-by-layer deposition of polymer has been achieved as well as molecular alignment along the writing direction of the cantilever. Many different functional polymers have been successfully deposited on silicon oxide substrates, including those that are temperature responsive, semiconducting, piezoelectric, and light-emitting, demonstrating that tDPN is a flexible nanolithography tool for polymer deposition and patterning. We will present our characterizations of the deposited polymers and report how tDPN can be used to optimize their properties. For example, poly(N-isopropylacrylamide) [pNIPAAm] nanostructures written by tDPN undergo a hydrophilic-to-hydrophobic phase transition induced by temperature that allows the structures to controllably capture and release proteins. We use carboxylic acid functionalized pNIPAAm as a tDPN "ink" that can be grafted onto an epoxy-terminated SAM substrate. We observe the temperature-dependent phase transition by monitoring the adhesion forces of the pNIPAAm with AFM. Finally, we will describe functional polymer patterns created by tDPN in ultra-high vacuum.

¹ Sheehan, et al., Appl. Phys. Lett. 85, 1589 (2004).

² Yang, et al., J. Amer. Chem. Soc. 128, 6774 (2006).

9:00am **NS-FrM4 Shadow Edge Lithography for Wafer-Scale Nanomanufacturing, J. Bai, J.-H. Chung, University of Washington**

Many upcoming applications, such as nanoelectronic circuitry, single-molecule based chips, nanofluidics, chemical sensors, and fuel cells, require large arrays of nanochannels and nanowires. The commercialization of these state-of-the-art nanostructure-based devices, which are far superior to the microdevices, is challenged by the patterning consistence, throughput, and cost. For the purpose, we propose the shadow edge lithography (SEL) as a silicon (Si) wafer-scale nanomanufacturing method. The shadow effect of "line-of-sight" in high-vacuum evaporation is theoretically analyzed to predict the geometric distributions of the nanoscale patterns. Nanoscale patterns are created by the shadow of aluminum (Al) edges that are prepatterned using a conventional microfabrication method. Feasibility of the method is demonstrated by the fabrication of nanoscale gaps, which are further used to fabricate either arrays of nanochannels or nanowires on 4-inch Si wafers. The fabricated nanogaps have widths ranging from 15 nm to 100 nm on the 4-inch Si wafers using an e-beam evaporator (NRC 3117, Varian Inc., Palo Alto, CA). Considering the virtual source during the e-beam evaporation, the experimental results agree well with the theoretical prediction. Furthermore, by using the height differences in the pre-patterned Al edges to compensate the geometric distributions of the shadow effect, it is found that the uniformity tolerance in nanogap width can be 2 nm or 5% across the entire 4-inch Si wafers at a resolution down to 20 nm. Upon the nanogap fabrication, arrays of nanochannels are fabricated by reactive ion etching (RIE) using the e-beam evaporated Al layers as the etching mask; or arrays of chromium (Cr) nanowires are fabricated by depositing 15-nm Cr layer on the nanogap patterns followed by an Al lift-off. The fabricated Cr nanowires are further used as the RIE mask to produce arrays of Si nanowires on silicon-on-insulator (SOI) wafers. Our results show that that the evaporated Al layers can be used as the RIE or lift-off mask to transfer the nanoscale patterns with clear configuration and high yield. Thus, the proposed SEL provides a robust method for wafer-scale manufacturing for sub 50-nm structures, which may exceed the performance of the other nanopatterning methods. Because of the parallel processing nature of the SEL, it has a potential to become a key technology for massive nanomanufacturing with cost effectiveness.

9:20am **NS-FrM5 Conformal Intermediate Layers for Anti-Adhesive Coatings on Metal Molds, H. Schift, Paul Scherrer Institute, Switzerland, S. Bellini, ETH Zürich, Switzerland, H. Sehr, J. Gobrecht, Paul Scherrer Institute, Switzerland**

Stamps for nanoimprint lithography (NIL)¹ need an excellent anti-sticking surface property, which is easy to achieve with silane chemistry, if molds are made from silicon.² Other stamp materials, such as metals, need intermediate layers, preferably made from silicon oxide (SiO₂).³ Then the chlorosilane group of commercially available fluorinated silanes can react with hydroxyl groups on the oxide surface under elimination of hydrochloric acid, and covalent binding can be achieved which is durable in hot embossing and injection molding processes. Two routes were developed to achieve a thin intermediate coating of stamps, one based on the thermal evaporation of Ti/SiO₂, and the other on Plasma Enhanced Chemical Vapor Deposition (PECVD) of SiO₂. Since evaporation is directed, a full conformal coverage of the surface, particularly if high aspect ratio structures need to be coated, is often only achieved with specific mounting setups or several subsequent coating steps from different directions. This is time consuming due to the evacuation steps and only results in limited thickness homogeneity. Therefore the PECVD was developed and applied on different metals (brass, nickel, steel) without the use of the Ti adhesion promoter. The process is conformal and 20 nm thick coatings can be achieved with high homogeneity. It is more flexible and can be performed within a few minutes. The most crucial point is the adhesion of the thin interlayer to the stamp surface during the demolding process. The durability of both layers was tested using different mechanical methods and coated molds were used in hot embossing and injection molding. Several thousand injection molding cycles are possible, and to date it seems that the durability of the new PECVD coating matches that of the evaporated films. This is a further step to establish anti-sticking coating techniques in high volume manufacturing of polymer parts by replication, and to enlarge the range of stamp materials used for molding and NIL.

¹ Schift H., Kristensen A., In Handbook of Nanotechnology, Vol. ed. B. Bhushan, second edition, Springer Verlag, Berlin, Germany, 239-278 (2007).

² Schift H., Saxer S., Park S., Padeste S., Pielas U., Gobrecht J., Nanotechnology 16, S171-S175 (2005).

³ Park S., Schift H., Padeste C., Schnyder B., Kötz K., Gobrecht J., Microelectronic Eng. 73-74, 196-201 (2004).

9:40am **NS-FrM6 Nanoscale Electron Beam Induced Etching (EBIE)**, *M.G. Lassiter, D. Smith*, University of Tennessee, *T. Liang*, Intel Corporation, *P.D. Rack*, University of Tennessee

Traditionally, high-resolution nanomachining utilizes a gallium focused ion beam (FIB) to physically sputter away material or dissociate a precursor material to deposit material. During the process, gallium ions are implanted into the surface of the substrate and leave undesirable effects, such as reduced transmission of clear area repairs in photomasks; otherwise damaging or change the remaining material. The use of electron beam induced processes for high spatial resolution nanopatterning has recently been developed as an alternative to FIB. The electron beam induces the dissociation of a precursor gas to cause a reaction at the surface of the material. This reaction either deposits material or removes material, depending upon the precursor/substrate combination. This presentation focuses on the latter, electron beam induced etching (EBIE) of materials. Electron beam induced etching provides superior spatial resolution and can offer much better etching selectivity compared to FIB. Additionally electrons do not damage the substrate materials because of their relatively small mass compared to gallium ions. This work characterizes the process of high resolution EBIE of various relevant materials. The effects of electron beam parameters such as accelerating voltage, beam current, and the scanning parameters are investigated, as well as the relationship of the beam parameters to the gas parameters such as pressure and injection needle position. Furthermore, various precursor gases were examined, and the effects on spatial resolution, etching rate, and selectivity against other materials are determined. A 3-D Monte Carlo type simulation of the etching process has also been developed and simulation results will be compared to experimental results.

10:00am **NS-FrM7 Atomic-Scale Device Fabrication in Silicon**, *M.Y. Simmons*, University of New South Wales, Australia **INVITED**

One driving force behind the microelectronics industry is the ability to pack ever more features onto a silicon chip, by continually miniaturising the individual components. However, after 2015 there is no known technological route to reduce device sizes below 10nm. In this talk we demonstrate a complete fabrication strategy towards atomic-scale device fabrication in silicon using phosphorus as a dopant in combination with scanning probe lithography and high purity crystal growth. A key aspect of being able to build single atom devices is the ability to distinguish single atoms on and in the silicon surface. We demonstrate a detailed understanding of the surface chemistry to identify and control individual P atoms, using phosphine as a dopant source in silicon.¹ We can place individual phosphorus atoms in silicon at precise locations² and encapsulate them in epitaxial silicon with minimal diffusion and segregation of the dopants.³ Separate studies have confirmed the range of electrical transport characteristics that can be achieved using phosphorus as a planar, buried dopant in the absence of any lithographic patterning by STM.⁴ We then demonstrate that we can pattern this planar dopant layer using STM lithography and encapsulate with low temperature silicon epitaxy without lateral diffusion of the dopants out of their lithographic regions. Electrical device characteristics at low temperatures confirm the presence of the lithographic patterning as we observe a cross-over from 2D to 1D transport in the phase coherence length.⁵ Using this process we have fabricated conducting nanoscale wires with widths down to ~8nm, tunnel junctions, single electron transistors and arrays of quantum dots in silicon.⁶ We will present an overview of the devices that have been made with this technology and highlight some of the challenges to achieving atomically precise devices.

¹ H.F. Wilson et al., Physical Review Letters 93, 226102 (2004).

² S. R. Schofield et al., Physical Review Letters 91, 136104 (2003).

³ K.E.J. Goh et al., Applied Physics Letters 85, 4953-4955 (2004).

⁴ K.E.J. Goh et al., Phys. Rev. B 73, 03541 (2006).

⁵ F.J. Rueß et al., Nano Letters 4, 1969 (2004).

⁶ F.J. Rueß et al., Small 3, 567 (2007); Nanotechnology 18, 044023 (2007); Phys. Rev. B Rapid 85, 121303 (2007).

10:40am **NS-FrM9 Advances in Atom Beam Nanolithography: A New Exposure Tool, Masks, and Resists**, *B. Craver, H. Guo, A. Roy*, University of Houston, *J. Strahan*, University of Texas, *J. Reynolds, H. Nounu*, University of Houston, *C.G. Willson*, University of Texas, *J.C. Wolfe*, University of Houston

Atom beam lithography (ABL) is a proximity printing technique where a broad beam of energetic neutral atoms floods a stencil mask and transmitted beamlets transfer the mask pattern to resist on a substrate. ABL exposures are equivalent to those formed by ions in every respect (mass, energy, angular distribution, diffraction, scattering within the mask, resist, and wafer) except for the charge of the lithography particles. ABL images, being formed by electrically neutral particles, are completely free of charge-related artifacts that occur, often unpredictably, in ion printing due to ambient electromagnetic fields and the buildup of electrostatic charge on the mask and wafer. In this paper, we describe an integrated toolset for

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fabricating high density arrays with an arbitrary unit cell by atom beam lithography. The 30-50 keV exposure tool incorporates a high brightness multicusp ion source and a high pressure gas cell to convert helium ions to energetic helium atoms through charge transfer scattering. A mechanical mechanism has been developed for translating the mask image over the wafer with 1 nm precision. Nano-arrays can, thus, be fabricated using a large-area template mask consisting of a silicon membrane with a periodic array of circular openings. The mask image is translated over the wafer to create, simultaneously, an array of identical unit cells, each corresponding to an individual mask opening. Silicon stencil masks, up to 700 nm thick, are fabricated with ~50 nm openings using a magnetically enhanced, molecular bromine plasma. A plasma-deposited coating of poly(methylmethacrylate) protects the silicon membrane from ion implantation damage and thickens the mask to enhance lithographic contrast. The mask can be coated with sputtered gold to shrink the mask openings as needed for the particular application. Pattern shifts during exposure are imperceptible at the nanometer-scale. Linewidths of 25 nm have been achieved and we anticipate reporting sub-20 nm linewidths at the conference. High resolution resists with optimized sensitivity, currently under development, will be reported at the conference. Potential applications in rapid prototyping and imprint lithography template fabrication will be discussed.

11:00am **NS-FrM10 Resonances in Secondary Electron Yields from Capped Multilayer Mirrors**, *E. Loginova, B. Yakshinskiy*, Rutgers University, *S. Yulin, T. Feigel*, Fraunhofer Institut (IOF), Germany, *J. Keister*, Brookhaven National Laboratory, *T. Lucatorto, C. Tarrío, S. Hill*, National Institute of Standards and Technology, *O. Dulub, U. Diebold*, Tulane University, *M. Chandok, M. Fang*, Intel Corporation, *T.E. Madey*, Rutgers University

The magnitude of secondary electron yield (SEY) at EUV wavelengths is a major factor in determining contamination rates of multilayer mirrors (MLMs) in EUV projection optics, and we have found striking resonance effects in measurements of SEY from MLMs. Low energy secondary electrons (0 to ~ 20 eV) can cause dissociation of adsorbed hydrocarbons from the background gas, and lead to carbon film growth on MLM surfaces. SEY data (electrons/photon) were measured using synchrotron radiation over the range 40 eV to 180 eV for TiO₂ and Ru single crystals (clean, O-covered, C-covered, air exposed) and compared with measurements for Mo/Si multilayer films capped by Ru, TiO₂, and RuO₂. For photon beams incident at 45 degrees, the shapes of the curves for Ru multilayers, especially the maxima at ~ 65 eV due to the Ru 4p excitation, are very similar to the data for pure Ru; such similarities are found also for a TiO₂ crystal and TiO₂-capped MLMs. Thus, the cap layer properties dominate the SEY characteristics: this agrees with theory, which predicts that a film several nm thick contributes ~90% to the SEY characteristics of the mirrors. For incidence angles close to the surface normal, and for photon energies near 92 eV (13.5 nm), dramatic energy- and angle-dependent resonances in SEY are observed for the capped MLMs, with SEYs 2 to 3 times higher than off-resonance. Calculations show excellent correlations between the photon electric field strength in the cap layers and the angular-dependent SEYs.

11:20am **NS-FrM11 Miniature Machines for Nano-Scale Research and Manufacturing: A New Model for Equipment and Instrumentation**, *M.L. Culpepper*, Massachusetts Institute of Technology **INVITED**

Advances in nanopositioning technology make it possible to (a) increase the pace of discoveries (via instruments) and (b) improve the pace with which discoveries are manufactured and commercialized. There are a growing number of instrument/equipment applications wherein small-scale (meso- and micro-scale) nanopositioners are needed in order to achieve commercially viable speeds (kHz), resolution (Angstroms), cost (\$100s) and thermal stability (Angstroms/min). New small-scale nanopositioners are emerging to meet these requirements, however there are a few technological issues that must be addressed. The purpose of this talk is to cover (i) the fundamental reasons that will compel the creation of these nanopositioners, (ii) the economic and performance benefits that they will enable and (iii) how partnerships can help to overcome the few remaining technical/scientific issues. The import of partnerships between machine design researchers, nanofabrication process researchers, and manufacturers will be stressed as well as a plan that is focused upon creating these partnerships. The talk ends with a vision for a new class of small-scale, low-cost instrument/equipment platforms to support a new model for nano-scale research and manufacturing.

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